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L13	(375/371.ccls.or 375/373.ccls. or 375/374.ccls. or 375/376.ccls.)	3510	L13
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L6	l3 and L5	0	L6
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L4	(phase near3 lock$3 near3 loop) and (frequenc$3 near3 lock$3 near3 loop$) and (current near3 convert$3) and (voltage near3 convert$3)	278	L4
L3	(phase near3 lock$3 near3 loop) same (frequenc$3 near3 lock$3 near3 loop$)	6846	L3
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END OF SEARCH HISTORY

L8: Entry 19 of 204 File: USPT Apr 14, 1998

DOCUMENT-IDENTIFIER: US 5740213 A
TITLE: Differential charge pump based phase locked loop or delay locked loop

YEAR FILED (1):
1994

Abstract Text (1):
A phase locked loop includes a differential charge pump to cancel static phase error and reduce sensitivity to noise. The differential charge pump comprises two substantially identical single-ended charge pumps so that under locked condition, changes in voltage at the charge pumps' output terminals are substantially identical, thereby maintaining a substantially constant difference between the charge pumps' output voltage. A differential input voltage-controlled oscillator receives the output of the differential charge pump and generates a clock signal with a frequency proportional to the voltage difference output by the differential charge pump. A common mode bias circuit adjusts the common mode voltage output by the differential charge pump to optimize the voltage swing available at the differential charge pump's output terminals. The structure can be easily modified to implement a delay locked loop by replacing the differential input voltage-controlled oscillator with a differential input voltage-controlled delay circuit.

Brief Summary Text (2):
This invention relates to phase locked loop and delay locked loop circuits, and more particularly, to phase locked loop and delay locked loop circuits incorporating differential charge pump circuits.

Brief Summary Text (4):
Phase locked loops and delay locked loops are routinely used for data communications, frequency synthesis, clock generation, clock recovery, and similar applications. Phase locked loops and delay locked loops are often implemented in integrated circuits and commonly are realized with charge pump techniques.

Brief Summary Text (5):
FIG. 1 shows a block diagram of a typical charge pump based phase locked loop 1. Phase locked loop 1 comprises a phase detector 4, a charge pump 5, a loop filter 7, and a voltage-controlled oscillator 9. Phase locked loop 1 operates to align clock signals in both frequency and phase.

Brief Summary Text (10):
Loop filter 7 is coupled at its input terminal 19 to output terminal 18 of charge pump 5. Loop filter 7 stabilizes the loop. Voltage-controlled oscillator 9 generates an oscillating output signal at CLKOUT terminal 13 whose frequency is proportional to the voltage at input terminal 20. Thus, when clock signal CLKI leads clock signal CLKO, voltage V.sub.CP increases as described above, which in turn causes voltage-controlled oscillator 9 to increase the frequency of clock signal CLKO. Conversely, when clock signal CLKI lags clock signal CLKO, voltage V.sub.CP decreases, which causes voltage-controlled oscillator 9 to decrease the frequency of clock signal CLKO. The feedback circuit of FIG. 1 thus constantly attempts to align clock signal CLKO with clock signal CLKI in frequency and phase. When the loop is substantially stabilized, clock signals CLKI and CLKO are aligned in frequency and phase and phase locked loop 1 is in the "locked" condition.

Brief Summary Text (11):
A delay locked loop operates in a similar manner to a phase locked loop except that the voltage controlled oscillator is replaced with a voltage controlled delay line.

The voltage controlled delay line receives clock signal CLKI and generates clock signal CLKO. The loop adjusts the delay in voltage controlled delay line until clock signals CLKI and CLKO are aligned in phase, which is the stabilized or locked condition.

Brief Summary Text (12):
Charge pump based phase locked loops and delay locked loops have some performance limitations. One such limitation is termed "static phase error". A static phase error is any phase error that exists between clock signals CLKI and CLKO under locked condition. Ideally, under locked condition, no static phase error should exist. However, in practice, circuit imperfections exist which cause a static phase error.

Brief Summary Text (14):
Another source of static phase error is the leakage current at output terminal 18 of charge pump 5 which causes changes in voltage V.sub.CP. Ideally, phase detector 4 does not generate any pulse on terminals 14 or 15 under locked condition. However, in practice, leakage current at output terminal 18 charges or discharges voltage V.sub.CP over time. As a result of the increase or decrease in voltage V.sub.CP, the action of phase locked loop 1 causes a change in the phase of clock signal CLKO. In the steady state, a static phase difference between clock signals CLKI and CLKO is introduced to cause charge pump 5 to substantially counteract effects of the leakage current at output terminal 18.

Brief Summary Text (15):
In some implementations, phase detector 4 generates a minimum pulse on each of terminals 14 and 15 of phase detector 4 to compensate for leakage currents in both the charging and discharging current sources in charge pump 5 when phase locked loop 1 is under locked condition. However, although minimum pulses on each of the terminals 14 and 15 compensate to some degree for the leakage current problem, at least four sources of static phase error result.

Brief Summary Text (16):
A first source of static phase error is unequal charge pump current sources. As mentioned above, charge pumps typically use a charging current source to charge output terminal 18 and a discharging current source to discharge output terminal 18. The charging current source and discharging current source are rarely exactly matched because of physical limitations. Thus, when a minimum pulse is forced on each of input terminals 16 and 17 of charge pump 5 under a locked condition, charge will be added or removed from output terminal 18 because the charging and discharging currents are not equal. This change in the charge at output terminal 18 causes a change in the voltage V.sub.CP, which in turn causes phase locked loop 1 to change the phase of clock signal CLKO thereby introducing a static phase error.

Brief Summary Text (17):
A second source of static phase error is unequal switching times. The charging and discharging current sources are selectably coupled to output terminal 18 by switches, which are invariably less than ideal. Switches for the charging and discharging current sources do not have identical switching times because of differences in type, sizes, bias conditions, drive, driver rise time and driver fall time, and other parametric values. Because the switching times of these switches are not identical, the charge transferred between the charging and discharging current sources and terminal 18 are not equal. Thus, charge will be added or removed from output terminal 18 when phase detector 4 forces the minimum pulse on input terminal 16 and input terminal 17 during lock. This change in the charge at output terminal 18 causes a change in voltage V.sub.CP, which in turn causes phase locked loop 1 to change the phase of clock signal CLKO, thereby introducing static phase error.

Brief Summary Text (20):
Another limitation of charge pump based circuits is sensitivity to any noise added to voltage V.sub.CP. Because voltage V.sub.CP controls the phase of clock signal CLKO, any noise added to voltage V.sub.CP will cause phase and frequency disturbances ("jitters") in clock signal CLKO. In many phase locked loop designs, clock signal CLKO is very sensitive to noise because the frequency of clock signal CLKO is designed to vary by a relatively large amount for a small change in voltage

V.sub.CP.

Brief Summary Text (24):
In accordance with one embodiment of the present invention, a phase locked loop is provided. The phase locked loop includes a differential charge pump to cancel static phase error and reduce sensitivity to noise. The differential charge pump comprises two substantially identical single-ended charge pumps so that, under locked condition, changes in voltage at the charge pumps' output terminals are substantially identical, thereby maintaining a substantially constant difference between the charge pumps' output voltages. In accordance with one embodiment of the present invention, a differential input voltage-controlled oscillator monitors the output of the differential charge pump and generates a clock signal having a frequency proportional to the output differential voltage of the differential charge pump. A common mode bias circuit adjusts the common mode voltage output of the differential charge pump to optimize the voltage swing available at the differential charge pump's output terminals.

Brief Summary Text (25):
In accordance with another embodiment of the present invention, a delay locked loop is provided. The structure is similar to one embodiment of the differential phase locked loop described above, except a differential voltage-controlled delay circuit is included in the delay locked loop instead of a voltage-controlled oscillator. The delay locked loop includes a differential charge pump to cancel static phase errors and reduce sensitivity to noise.

Drawing Description Text (2):
FIG. 1 shows a block diagram of a typical charge pump based phase locked loop 1.

Drawing Description Text (5):
FIG. 3 shows a block diagram of a differential charge pump based phase locked loop 300 according to one embodiment of the present invention.

Drawing Description Text (11):
FIG. 7 shows a circuit diagram of one embodiment of the voltage-to-current converter 50 depicted in FIG. 5.

Drawing Description Text (14):
FIG. 9 shows a block diagram of a second embodiment of a differential charge pump based phase locked loop 900 according to the present invention.

Detailed Description Text (2):
FIG. 3 shows a block diagram of a differential charge pump phase locked loop 300 according to one embodiment of the present invention. Hereinafter, where elements function substantially the same as elements in prior figures, the same reference numerals are employed. Phase locked loop 300 includes a phase detector 104, a differential charge pump formed from charge pumps 5 and 5a, a loop filter 7, a loop filter 7a, a common mode bias circuit 80 and a voltage-controlled oscillator 70.

Detailed Description Text (3):
Phase detector 104 of phase locked loop 300 receives clock signals CLKI and CLKO at terminals 11 and 12, respectively. When clock signal CLKI leads clock signal CLKO, phase detector 104 generates a pulse on output terminal 14. This pulse causes charge pump 5 to add charge to output terminal 18, thereby increasing voltage V.sub.CP+. At the same time, this pulse causes charge pump 5a to remove charge from output terminal 18a thereby decreasing voltage V.sub.CP-. As a result, the difference between voltages V.sub.CP+ and V.sub.CP- is increased. Loop filters 7 and 7a stabilize the loop. Voltage-controlled oscillator 70 detects the increased voltage difference between voltages V.sub.CP+ and V.sub.CP- and increases the frequency of clock signal CLKO to align clock signal CLKO to clock signal CLKI. Phase locked loop 300 constantly attempts to align clock signal CLKO with clock signal CLKI in frequency and phase.

Detailed Description Text (13):
FIG. 6 shows a block diagram of a differential voltage-controlled oscillator 70 in accordance with one embodiment of the present invention. Differential

voltage-controlled oscillator 70 includes a voltage-to-current converter 50, a capacitor 52, a comparator 53, and switches 55, 56 and 57. Voltage-to-current converter 50 further includes a dependent current source 51.

Detailed Description Text (14):
Voltage-to-current converter 50 receives the voltages V.sub.CP+ and V.sub.CP- at input terminals 71 and 72 and provides a current at terminal 54 proportional to a voltage difference .DELTA.V.sub.IN between terminals 71 and 72. The current provided by voltage-to-current converter 50 to terminal 54 is used to charge capacitor 52.

Detailed Description Text (15):
During operation, the signal generated by comparator 53 at node 58 is either at a logic "one" or logic "zero" voltage level. When the signal generated by comparator 53 is a logic "one", switches 55 and 56 are closed, and switch 57 is open. As a result, switch 55 couples node 59 to GROUND and discharges capacitor 52, thereby causing a decreasing voltage on node 59. Switch 56 couples a voltage V1 to a node 60 at the V-terminal of comparator 53. Thus, comparator 53 compares the decreasing voltage on node 59 to voltage V1. When the voltage on node 59 drops below voltage V1, comparator 53 generates a logic "zero" voltage level at node 58, which is connected to CLKOUT terminal 13. The logic "zero" voltage level at node 58 opens switches 55 and 56 and closes switch 57. When switch 55 is open, voltage-to-current converter 50 charges capacitor 52, thereby increasing voltage on node 59. Because switch 56 is open and switch 57 is closed, a voltage V2 is coupled to the V-terminal of comparator 53. Consequently, comparator 53 compares the increasing voltage on node 59 to voltage V2. When the voltage on node 59 rises above voltage V2, comparator 53 generates a logic "one" voltage level at node 58, which is connected to CLKOUT terminal 13. The charging and discharging cycles of capacitor 52 repeats indefinitely so that comparator 53 generates clock signal CLKO at CLKOUT terminal 13.

Detailed Description Text (18):
FIG. 7 shows a circuit diagram of one embodiment of voltage-to-current converter 50. In FIG. 7, Voltage V.sub.CP+ is provided on the gate of N-channel transistor 91, and voltage V.sub.CP- is provided on the gate of N-channel transistor 92. Transistor 91 and current source 97 form a source follower circuit so that the voltage at node 94 is proportional to voltage V.sub.CP+. Likewise, transistor 92 and current source 98 form a source follower circuit so that the voltage at node 95 is proportional to voltage V.sub.CP-. When voltages V.sub.CP+ and V.sub.CP- are equal (i.e., when phase locked loop 300 is in locked condition), the voltages at nodes 94 and 95 are equal because transistors 91 and 92 are substantially identical and both conduct current I.sub.1. Consequently, when voltage V.sub.CP+ rises relative to voltage V.sub.CP-, the voltage at node 94 rises relative to the voltage at node 95, causing current .DELTA.I, proportional to the difference between voltages V.sub.CP+ and V.sub.CP-, to flow from node 94, through node 96 and resistors 93 and 93a, to node 95. As a result, transistor 91 conducts current I which is equal to I.sub.1 +.DELTA.I. The current in N-channel transistor 91 also flows in P-channel transistor 90 and is mirrored to P-channel transistor 51 so that a current I is also conducted in transistor 51. Consequently, P-channel transistor 51 also conducts a current I.sub.1 +.DELTA.I, which is output to terminal 54 through diode connected transistor 101. In some embodiments, diode connected transistor 101 is optional.

Detailed Description Text (20):
FIG. 8 shows a block diagram of common mode bias circuit 80 (FIG. 3) according to one embodiment of the present invention. During operation of phase locked loop 300 (FIG. 3), the voltage difference between voltage V.sub.CP+ and voltage V.sub.CP- on the charge pump output terminals 18 and 18a (FIG. 3), respectively, is forced to the differential voltage required to make clock signals CLKI and CLKO equal in frequency and phase. However, the common mode voltage on output terminals 18 and 18a is not affected by the loop. Common mode bias circuit 80 adjusts the common mode voltage on output terminals 18 and 18a and sets the common mode voltage to optimize the voltage swing available at the output terminals 18 and 18a.

Detailed Description Text (23):
The differential scheme implemented in phase locked loop 300 reduces the static phase error to near zero under locked condition through cancellation of errors. In

the embodiment discussed above, matched current sources in a charge pump are used. In practice, current sources within a charge pump are difficult to match; however, two charge pumps can be matched very closely. Phase locked loop 300 generates a minimum pulse on each of phase detector output terminals 14 and 15 when phase locked loop 300 is under locked condition to reduce static phase error caused by leakage currents at charge pump output terminals 18 and 18a. Substantial cancellation of the resulting four error sources described above for phase locked loop 1 occurs because charge pumps 5 and 5a are manufactured to be substantially identical to each other, and loop filters 7 and 7a are manufactured to be substantially identical to each other.

Detailed Description Text (26):
Yet another advantage of phase locked loop 300 over typical phase locked loop 1 is that the effective voltage range on the charge pump output terminals 18 and 18a is doubled because the differential charge pump circuit (i.e. the circuit which includes charge pumps 5 and 5a) provides a differential voltage to differential voltage-controlled oscillator 70. That is, the maximum voltage range of voltages V.sub.CP+ and V.sub.CP- is twice that of voltage V.sub.CP in phase lock loop 1 because the differential voltage seen by voltage-controlled oscillator 70 is twice what is seen by voltage-controlled oscillator 9.

Detailed Description Text (27):
FIG. 9 shows a block diagram of a second embodiment of a phase locked loop according to the present invention. Phase locked loop 900 is similar to phase locked loop 300 (FIG. 3), but differs from phase locked loop 300 in the implementation of differential voltage-controlled oscillator 170 and common mode bias circuit 180. Differential voltage-controlled oscillator 170 comprises voltage-to-current converter 50 and ring oscillator 110. The speed at which ring oscillator 110 operates is controlled by the current generated by voltage-to-current converter 50. Similar to phase locked loop 300, phase locked loop 900 employs a differential scheme to reduce static phase errors under locked condition through cancellation of errors.

Detailed Description Text (28):
In this embodiment, voltage-to-current converter 50 generates the common mode voltage V.sub.CM. As discussed above in conjunction with FIG. 7, voltage V.sub.CM is generated by voltage-to-current converter 50 and output at terminal 103, which is coupled to node 123 of common mode bias circuit 180 (FIG. 9). Referring back to FIG. 7, transistor 91 and current source 97 form a source follower circuit. As a result, the voltage on node 94 approximates the voltage on the gate of transistor 91, V.sub.CP+ minus the threshold voltage of transistor 91. Similarly, transistor 92 and current source 98 form a source follower circuit and, thus, the voltage on node 95 approximates V.sub.CP- minus the threshold voltage of transistor 92. Transistors 91 and 92 are designed so that their threshold voltages are substantially identical, and resistors 93 and 93a are designed to have substantially equal resistances. As a result, the voltage at node 96 is substantially at the midpoint between the voltages at nodes 94 and 95. Thus, the voltage at node 96 (and terminal 103) is substantially equal to the average of voltages V.sub.CP+ and V.sub.CP-, minus a threshold voltage.

Detailed Description Text (29):
FIG. 10 shows a block diagram of ring oscillator 110 depicted in the differential phase locked loop 900 of FIG. 9. Ring oscillator 110 is an eight stage oscillator formed by substantially identical stages 111a-111h. Unlike differential voltage-controlled oscillator 70 of FIG. 6, in differential voltage-controlled oscillator 170, terminal 54 of voltage-to-current converter 50 (FIG. 7) is coupled to GROUND rather than a terminal of capacitor 52. In the embodiment of FIG. 9, voltages V.sub.P from node 100 and V.sub.N from node 102 of voltage-to-current converter 50 (FIG. 7) are coupled to terminals 112a and 113a of ring oscillator 110's stage 111a, respectively. As shown in FIG. 10, in stages 111b-111h, the input V.sub.I+ and V.sub.I- nodes are connected to the output V.sub.O+ and V.sub.I- nodes of the previous stage in the ring, respectively. In stage 111a, V.sub.I+ node 115a and V.sub.I- node 116a are connected to the V.sub.O- node 118h and V.sub.O+ node 117h of stage 111h, respectively. When the output signal of stage 111a is a logic "one", stage 111b generates a logic "one" output signal, which in turn causes stage

111c to generate a logic "one" output signal, and so on to stage 111h. Then when stage 111h generates a logic one output signal, stage 111a generates a logic "zero" output signal because the polarities of the output voltages of stage 111h are connected to stage 111a's input terminals of opposite polarities. The logic "zero" signal is then propagated through the ring to stage 111h. In this manner, alternating logic "zero" and logic "one" signals are propagated through ring oscillator 110 indefinitely. In this embodiment, node 117h provides level shifter 119 at input terminal 120 voltage V.sub.O+ to generate a 5 volt clock signal at output terminal 73.

Detailed Description Text (30):
FIG. 11 shows a circuit diagram of one embodiment of one stage of the ring oscillator of FIG. 10. Terminal 112 is connected to node 100 of voltage-to-current converter 50 (FIG. 7). P-channel transistors 120 and 121 which are controlled by the voltage of terminal 112, hence each conduct current I mirrored from transistor 51 in voltage-to-current converter 50 (FIG. 7).

Detailed Description Text (31):
N-channel transistors 123 and 124 operate as switches controlled by the voltages at nodes 115 and 116, respectively. Thus, when the voltage at V.sub.I+ terminal 115 transitions from logic "one" to logic "zero" (thus, the voltage at V.sub.I- terminal transistors from logic "zero" to logic "one") transistor 123 is forced to the "OFF" state and transistor 124 is forced to the "ON" or conducting state. In the conducting state, transistor 124 conducts current I of transistor 124 to the drain terminal of N-channel transistor 125. The gate terminal of transistor 125 is connected to terminal 113, which is connected to node 102 of voltage-to-current converter 50. Because the source of transistor 101 (FIG. 7) is connected to GROUND in this embodiment, the current in transistor 125 is mirrored from transistor 101 in voltage-to-current converter 50 (FIG. 7). Transistor 125 is designed to have twice the width-to-length ratio of transistor 101 so that transistor 125 conducts a current which is twice the current in transistor 101. Consequently, when transistor 124 is conducting, transistor 125 pulls down the voltage at node 126, until the voltage at node 126 drops to one threshold voltage of transistor 134 below voltage V.sub.CL- (impressed at the gate and drain terminals of transistor 134). At that voltage, transistor 134 begins to conduct, thereby clamping the voltage at node 126 substantially at one threshold voltage (V.sub.T) below voltage V.sub.CL-. As a result, the voltage at V.sub.O+ terminal 117 approximates V.sub.CL- -V.sub.T. The speed at which the voltage at node 126 is pulled down is directly related to the size of the current conducted by transistor 125. Consequently, when the current conducted by transistor 101 increases, the voltage at node 126 is pulled down faster, thereby causing ring oscillator 110 to operate faster. Conversely, when the current conducted by transistor 101 decreases, the voltage at node 126 is pulled down more slowly, thereby causing ring oscillator 110 to operate more slowly.

Detailed Description Text (33):
Similarly, when the voltage at V.sub.I+ node 115 transitions from logic "zero" to logic "one" (and thus, the voltage at V.sub.I- node 116 transitions from logic "one" to logic "zero"), transistor 123 is forced to the "ON" state and transistor 124 is forced to the "OFF" state. Because transistor 123 is in the "ON" state, transistor 125 pulls down the voltage at node 127, which is clamped substantially at one threshold voltage below voltage V.sub.CL-. Meanwhile, because transistor 124 is in the "OFF" state, transistor 121 charges node 126, thereby increasing the voltage at node 126, which is clamped substantially at one threshold voltage above voltage V.sub.CL+. Similar to the discussion above, the current conducted by transistors 51 and 101 in voltage-to-current converter 50 (FIG. 7) control the rates at which node 127 is pulled down and node 126 is charged. Because voltage-to-current converter 50 (FIG. 7) controls the current conducted by transistors 51 and 101, voltage-to-current converter 50 also controls the speed at which ring oscillator 110 operates.

Detailed Description Text (34):
FIG. 12 shows a circuit diagram of one embodiment of the common mode bias circuit 180 depicted in FIG. 9. Common mode bias circuit receives common mode voltage V.sub.CM at node 123 from terminal 103 of voltage-to-current converter 50 (FIG. 7). Amplifier 88 monitors voltage V.sub.CM and voltage V.sub.REF generated by voltage

generator 181, and outputs a voltage that is a function of the difference between V.sub.CM and V.sub.REF. When V.sub.CM is equal to V.sub.REF, transistors 85 and 85a each conduct substantially the same current as current sources 84 and 84a, respectively. When V.sub.CM is greater than V.sub.REF, amplifier 88 increases the voltage impressed at the gates of transistors 85 and 85a, thereby causing transistors 85 and 85a to conduct more current, which pulls down the voltages at terminals 81 and 82. Similarly, when V.sub.CM is less than V.sub.REF, amplifier 88 decreases the voltage impressed at the gates of transistors 85 and 85a, thereby causing transistors 85 and 85a to conduct less current, which pulls up the voltages at terminals 81 and 82. Common mode bias circuit 180 operates continuously in this manner to adjust V.sub.CM in the direction of decreasing the difference between voltages V.sub.CM and V.sub.REF until they are substantially equal.

Detailed Description Text (35):
Voltage generator 181 includes current sources 183 and 199, transistors 185 and 186, and resistors 193 and 193a and operates to generate reference voltage V.sub.REF that optimizes the voltage range of voltages V.sub.CP+ and V.sub.CP-. This embodiment of voltage generator 181 is used when current source 97 and 98 in voltage-to-current converter 50 (FIG. 7) are N-channel transistors.

Detailed Description Text (38):
Current source 199 is designed to conduct current I.sub.1 and thus, diode connected transistor 185 also conducts current I.sub.1. Transistors 185 and 186 have their sources connected to ground potential and thus, have the same source potential. The gate of transistor 186 is connected to the gate of transistor 185, and has a width-to-length ratio approximately 1.4 times larger than the width-to-length ratio of transistor 185. Because transistors 185 and 186 have the substantially the same source potential, gate potential and drain current, but transistor 186's width-to-length ratio is approximately 1.4 times larger, transistor 186 operates in the linear region resulting in a drain potential proportional to the saturation voltage of the transistor implementing current source 98 (FIG. 7). The drain potential of transistor 186 substantially tracks the variations in the saturation voltage of the transistor implementing current source 98 (FIG. 7) caused by temperature, process, and power supply voltage variations. Accordingly, the voltage at node 196 is approximately the same as voltage V.sub.CM when the voltage at node 95 (FIG. 7) is at the saturation voltage. Because voltage generator 181 includes resistors and current sources substantially identical to resistors and current sources in voltage-to-current converter 50 (FIG. 7), the reference voltage substantially identically tracks variations in the saturation voltage due to temperature, process variations and power supply changes. As a result, common mode bias circuit 180 adjusts the common mode voltage to a level to optimize the voltage swing available on the charge pump output terminals 18 and 18a.

Detailed Description Text (40):
FIG. 13 shows a block diagram of one embodiment of a delay locked loop 1300 according to one embodiment of the present invention. Delay locked loop 1300 is substantially the same as phase locked loop 900 except that Delay locked loop 1300 has a voltage-controlled delay circuit 1310 instead of voltage-controlled oscillator 170 as in phase locked loop 900. Voltage-controlled delay circuit 1310 includes voltage-to-current converter 50, which is coupled to delay circuit 1320 instead of ring oscillator 110. The other elements of delay locked loop 1300 are substantially the same as in phase locked loop 900. It is appreciated that delay locked loop 1300 employs a differential scheme as described above for phase locked loop 300, thereby reducing static phase error through cancellation of errors.

Detailed Description Text (41):
Except as noted above, all the elements common to delay locked loop 1300 and phase locked loop 900 are connected and function in substantially the same manner as described above. As described above for phase locked loop 900: phase detector 104 detects the phase difference between clock signals CLKI and CLKO and generates pulses at terminals 14 and 15; charge pumps 5 and 5a control the voltages V.sub.CP+ and V.sub.CP- in response to the pulses generated by phase detector 104; loop filters 7 and 7a stabilize the loop; common mode bias circuit 180 adjusts the common mode voltage to maximize the voltage swing of voltages V.sub.CP+ and V.sub.CP- ; and voltage-to-current converter 50 generates a current proportional to the difference

between voltages V.sub.CP+ and V.sub.CP-.

Detailed Description Text (42):
Delay circuit 1320 receives clock signal CLKI at terminal 115a and voltages V.sub.P and V.sub.N generated by voltage-to-current converter 50 at terminals 112a and 113a, respectively. Delay 1320 generates clock signal CLKO at terminal 115h. Delay circuit 1320 aligns the phase of clock signal CLKO with clock signal CLKI by varying the delay experienced by clock signal CLKO in delay circuit 1320 in proportion to the difference between voltages V.sub.CP+ and V.sub.CP-.

Detailed Description Text (43):
FIG. 14 shows a block diagram of one embodiment of the delay circuit 1320 depicted in FIG. 13. Delay circuit 1320 is basically ring oscillator 110 (FIG. 10) with the ring "broken" and clock signal CLKI connected to terminal 115a. Clock signal C1KI is inverted and connected to terminal 116a. As a result, each transition of clock signal CLKI propagates through stages 111a-111h, thereby generating clock signal CLKO. The rate at which each transition of clock signal CLKI propagates through delay circuit 1320 is controlled by the speed at each stage transitions from one logic state to the opposite logic state. As stated in the discussion above for FIG. 11, the currents conducted by transistors 51 and 101 of voltage-to-current converter 50 (FIG. 7) control the speed at which each stage 111a-111h transitions. Thus, the voltage difference between voltages V.sub.CP+ and V.sub.CP-. controls the speed at which each stage 111a-111h transitions, thereby adjusting the delay through delay circuit 1320 to align clock signal CLKO with clock signal CLKI.

Other Reference Publication (1):
Robert R. Cordell et al., "A 50 MHz Phase-and Frequency-Locked Loop," IEEE Journal of Solid-State Circuits, vol. SC-14, No. 6, Dec. 1979, pp. 1003-1009.

Other Reference Publication (5):
Floyd M. Gardner, "Charge-Pump Phase-Lock Loops," IEEE Transactions on Communications, vol. COM-28, No. 11, Nov. 1980, pp. 1849-1858.

CLAIMS:

6. A circuit for aligning a phase of a first signal and a second signal comprising:

a differential charge pump circuit having a first input terminal, a second input terminal, a first output terminal and a second output terminal, wherein said differential charge pump circuit generates at said first output terminal and said second output terminal a differential signal in response to a phase difference between said first signal and said second signal; and

a differential input voltage-controlled oscillator circuit coupled to said first output terminal and said second output terminal of said differential charge pump circuit, wherein:

said differential input voltage-controlled oscillator circuit generates an output signal having a frequency proportional to said differential signal generated by said differential charge pump circuit, said output signal of said voltage-controlled oscillator being said second signal; and

said differential input voltage-controlled oscillator further comprises a differential input voltage-to-current converter for providing an output current proportional to said differential signal generated by said differential charge pump circuit.

13. The circuit recited in claim 6, wherein said differential input voltage-controlled oscillator further comprises a ring oscillator coupled to said differential input voltage-to-current converter, said ring oscillator generating said output signal of said differential input voltage-controlled oscillator having a frequency proportional to said output current provided by said differential input voltage-to-current converter.

20. The circuit recited in claim 19 wherein, said voltage-controlled delay circuit

further comprises a differential input voltage-to-current converter.

L2: Entry 3 of 19 File: USPT Nov 9, 1999

DOCUMENT-IDENTIFIER: US 5982242 A
TITLE: Circuit for synchronizing transmission local oscillating frequencies in digital microwave system

Brief Summary Text (10):
The following patents each disclose features in common with the present invention but do not teach or suggest the specifically recited circuit for synchronizing transmission local oscillating frequencies and a digital microwave system as in the present invention: U.S. Pat. No. 5,592,126 to Boudewijns et al., entitled Multiphase Output Oscillator, U.S. Pat. No. 4,598,257 to Southard, entitled Clock Pulse Signal Generator System, U.S. Pat. No. 4,779,008 to Kessels, entitled Multiple Redundant Clock System Comprising A Number Of Mutually Synchronizing Clocks, And Clock Circuit For Use In Such A Clock System, U.S. Pat. No. 5,233,315 to Verhoeven, entitled Coupled Regenerative Oscillator Circuit, U.S. Pat. No. 5,301,171 to Blow et al., entitled Cross-Monitored Pair Of Clocks For Processor Fail-Safe Operation, U.S. Pat. No. 4,025,874 to Abbey, entitled Master/Slave Clock Arrangement For Providing Reliable Clock Signal, U.S. Pat. No. 5,059,926 to Karczewski, entitled Frequency Synchronization Apparatus, U.S. Pat. No. 5,422,604 to Jokura, entitled Local oscillation Frequency synthesizer For Vibration Suppression In The Vicinity Of A Frequency Converging Value, U.S. Pat. No. 5,675,620 to Chen, entitled High-Frequency Phase Locked Loop Circuit, U.S. Pat. No. 5,610,558 to Mittel et al., entitled Controlled Tracking Of Oscillators In A Circuit With Multiple Frequency Sensitive Elements, U.S. Pat. No. 5,657,359 to Sakae et al, entitled Phase Synchronizer And Data Reproducing Apparatus, and U.S. Pat. No. 5,359,298 to Abe, entitled VCO Having Voltage-To-Current Converter And PLL Using Same.

L15: Entry 6 of 8 File: USPT May 9, 1995

DOCUMENT-IDENTIFIER: US 5414390 A
TITLE: Center frequency controlled phase locked loop system

Abstract Text (1):
A center frequency controlled phase locked loop system includes a primary phase locked loop having a first voltage controlled oscillator including a first voltage to current converter whose output current drives a first current controlled oscillator to produce the primary clock signal to be locked onto an input signal; a second phase locked loop having a second voltage controlled oscillator including a second voltage to current converter whose output current drives a second current controlled oscillator to produce the synthesized clock signal whose frequency is approximately that of the input signal or integral multiple thereof; and a current copier circuit for copying the output current from the second voltage to current converter and delivering it to the first current controlled oscillator to maintain the center frequency of the first voltage controlled oscillator at approximately the output frequency of the synthesized clock signal.

Brief Summary Text (13):
This invention features a center frequency controlled phase locked loop system. There is a primary phase locked loop having a first voltage controlled oscillator including a first voltage to current converter whose output current drives a first current controlled oscillator to produce the primary clock signal to be locked onto an input signal. A second phase locked loop has a second voltage controlled oscillator including a second voltage to current converter whose output current drives a second current controlled oscillator to produce the synthesized clock signal whose frequency is approximately that of the input signal or an integral multiple thereof. A current copier circuit copies the output current from the second voltage to current converter and delivers it to the first current controlled oscillator to maintain the center frequency of the first voltage controlled oscillator at approximately the output frequency of the synthesized clock signal.

Brief Summary Text (14):
In a preferred embodiment the current copier circuit may include a sample and hold circuit. The current copier circuit may include a control circuit such as the switching elements included in the sample and hold circuit for fixing the current supplied from the second voltage to current converter to the first current controlled oscillator when the primary phase locked loop is locking onto an input signal such as for example when a read signal is being acquired from a disk drive.

Detailed Description Text (2):
In accordance with this invention the frequency of VCO can be easily, adjustably, continually kept within 20% of the synthesizer clock signal on line 32 and in fact can be kept to within 1 or 2% of that signal and so within 1 or 2% of the frequency of the read data signal on line 42. VCO1 56, FIG. 2, includes voltage to current converter 70 and current controlled oscillator 72. Voltage controlled oscillator VCO2 30 in secondary loop 14 also includes a voltage to current converter 74 and current controlled oscillator 76.

Detailed Description Text (3):
It is a realization of this invention that since the current supplied from voltage to current converter 74 to current controlled oscillator 76 is a current which provides a synthesizer clock signal on line 32 which is within 1 or 2% of the expected frequency of the read data signal on line 42 that this same current could be copied in current copier circuit 80 and delivered to control the center frequency current of current controlled oscillator 72. In this way the VCO clock output on

line 48 from current controlled oscillator 72 would not only be within 1 or 2% instead of 20% of the synthesizer clock and read data signal frequencies, but it would also be controlled in real time. That is, any time the synthesizer clock signal frequency changed in order to accommodate an expected change in the read data signal frequency or in accommodating time or voltage drift, the center frequency of current controlled oscillator 72 would be changed automatically accordingly. Current copier circuit 80 may be implemented as shown by a sample and hold circuit 82.

Detailed Description Text (4):
Since sample and hold circuit 82 includes switching means, it may perform intrinsically as a control circuit for fixing the current supplied from the second voltage to current converter 74 to the first current controlled oscillator 72. That is, whenever a read gate signal occurs, sample and hold circuit 82 is made to hold the particular value stored in it at that moment and maintain that value as the input to current controlled oscillator 72 during the duration of the read operation. This is done so that during the read operation only the incoming read data signal on line 42 will control the frequency of loop 12; otherwise there would be two signals.

Detailed Description Text (5):
The operation of current copier 80 utilizing sample and hold circuit 82 is shown in greater detail in FIG. 3. FET 90 in voltage to current converter VCO2 74 controls the current controlled oscillator ICO2 76. The voltage V.sub.b on the gate of FET 90 is mirrored at the gate of FET 92 in copier 80 to create an identical current, here called I.sub.CF to drive current to voltage converter 72. Since both current to voltage converters 76 and 72 are identical in terms of their process and fabrication, the same current applied to both will cause both circuits to provide the same output frequency within a few percent. When it is desired to read the associated disk, a read gate signal opens switch 94 in sample and hold circuit 82 so that capacitor C 96 stores the voltage then present and maintains that voltage on the gate of FET 92 during the entire read operation, so that it is only the frequency of the read signal which is affecting the frequency of the phase locked loop system.

Current US Cross Reference Classification (5):
375/376

CLAIMS:

1. A center frequency controlled phase locked loop (PLL) system, comprising:

a primary PLL having a first voltage controlled oscillator including a first voltage to current converter whose output current drives a first current controlled oscillator to produce the primary clock signal to be locked on to an input signal;

a second PLL having a second voltage controlled oscillator including a second voltage to current converter whose output circuit drives a second current controlled oscillator to produce the synthesized clock signal whose frequency is approximately that of the input signal or an integral multiple thereof; and

a current copier circuit for copying the output current from said second voltage to current converter and delivering it to said first current controlled oscillator to maintain the center frequency of said first voltage controlled oscillator at approximately the output frequency of said synthesized clock signal.

3. The center frequency controlled phase locked loop system of claim 1 in which said current copier circuit includes a control circuit for fixing the current supplied from said second voltage to current converter to said first current controlled oscillator when said primary PLL is locking on to an input signal.

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Generate Collection

L15: Entry 1 of 8 File: USPT Feb 25, 2003

DOCUMENT-IDENTIFIER: US 6526111 B1
TITLE: Method and apparatus for phase locked loop having reduced jitter and/or frequency biasing

Detailed Description Text (12):
FIG. 3 illustrates a schematic block diagram of the controlled oscillator 18 that includes a biasing circuit 60. The controlled oscillator 18 is implemented as a voltage control oscillator. As such, it includes a voltage to current converter 68. In addition, the controlled oscillator includes the biasing circuits 60, a plurality of transistors, Q9 through Q13, a plurality of resistors, R1 and R2 and a ring oscillator 66. The biasing circuit 60 includes a reference current source 64, a monitoring circuit 62, a plurality of transistors Q1 through Q7, and a plurality of resistors R3 and R4.

Detailed Description Text (13):
In start up conditions, or large transitions in output frequency selections, the biasing circuit is active. Otherwise, the biasing circuit is inactive having negligible effect on the overall operation of the phase lock loop. During start up conditions, the representative signal is low. As such, the voltage across R1 and R2 is low and little or no current is flowing through Q9. To provide biasing, when the output of the voltage to current converter 68 is low, Q3 through 7 are off and Q1 and 2 are on. With Q1 active, a biasing current that substantially matches the referenced current produced by reference current source 64 is flowing through transistors Q12 and Q13. As such, a current and/or voltage is applied to the ring oscillator 66 thereby producing a minimum frequency output signal 34. As the output of the current to voltage converter increases, but remains below a threshold of the biasing circuit (e.g., 10 nanoamps to several microamps), has Q1 through Q7 in an active state. In addition, as the output of the current to voltage converter is increasing Q9 and Q10 are becoming active. Thus, the current I.sub.VCO through transistors Q12 and Q13 equal the summation of the bias current. As such, the output frequency of the ring oscillator is increasing from the minimum output frequency, which is established via the referenced current source 64.

Detailed Description Text (14):
Once the threshold is exceeded, Q3 through Q7 are active. With Q3 active, Q1 and Q2 are off. When Q1 is off, the biasing current is zero such that I.sub.VCO equals the current through Q9. Thus, the current through Q9 equals the voltage at the output of the current to voltage converter divided by the resistance of R2.

Current US Original Classification (1):
375/376

Current US Cross Reference Classification (2):
375/374

L7: Entry 34 of 39 File: USPT Apr 30, 1996

DOCUMENT-IDENTIFIER: US 5512860 A
TITLE: Clock recovery phase locked loop control using clock difference detection and forced low frequency startup

Abstract Text (1):
A method of generating output clock pulses using a phase locked loop which includes a voltage controlled oscillator (VCO) is comprised of providing a sequence of data pulses and a sequence of reference clock pulses, resetting the phase locked loop to force the VCO to its lowest operating frequency, releasing reset of the phase locked loop and forcing the VCO to lock to a multiple of the frequency of the reference clock pulses, detecting the presence of data pulse transitions, in the event of detection of data pulse transitions, forcing the VCO to lock to the data pulses, and outputting output clock pulses from the phase locked loop.

Brief Summary Text (2):
This invention relates to digital transmission systems and in particular to a clock recovery circuit which uses a phase locked loop.

Brief Summary Text (4):
False locking occurs when a phase locked loop locks to a frequency other than that of a data stream from which a clock signal is to be recovered. False locking to harmonics (e.g. half or double) of the data stream baud rate sometimes occurs. False locking can also occur at other frequencies which are closer to the baud rate of the data stream. This occurs because a standard phase detector used for recovery of clock from a data stream may not drive a phase locked loop to lock if the phase locked loop voltage controlled oscillator (VCO) and the data stream differ in frequency by more than a small amount. This difference is typically much less than the total frequency range of the VCO. This is normally the case with VCOs that are implemented in very large integrated circuits (VLSI) because such VCOs must have a wide frequency range to ensure that across variations in process, voltage and temperature, the VCO range always encompasses the frequency of data streams from which the clock frequency and phase is to be recovered. A discussion of "false locking" can be found in the paper "The Applications of Linear Servo Theory to the Design of AGC Loops", by W. K Victor in Proceedings of the IRE, Vol 48, February 1960.

Brief Summary Text (5):
Existing systems typically use one of two approaches to avoid false locking. The first approach is to tune or trim the VCO such that its total frequency range is limited and is centered about the frequency of the data stream to be recovered. If the VCO is restricted sufficiently, this ensures that the phase detector is always able to drive the phase locked loop into lock. A disadvantage of this approach is the production cost of tuning or trimming the VCO frequency range. For low cost, highly manufacturable products such an approach is not viable.

Brief Summary Text (6):
The second approach to avoid false locking is to train the phase locked loop using a phase/frequency detector that locks the phase locked loop to a clock (typically provided by a crystal oscillator) that is known to be very closely related to the frequency of the data stream to be recovered. To reduce costs, the reference crystal used is usually an integer submultiple of the data stream baud rate. For example, when recovering 155.56 MHz, a 19.44 MHz reference crystal can be used for training the phase locked loop (which is 1/8 the nominal frequency of the clock to be recovered).

Brief Summary Text (8):
A typical case under which a phase locked loop may drift significantly from its nominal frequency is during a loss of signal event. For example, loss of signal occurs when a cable or fiber carrying the received data stream is cut. To detect loss of signal, many clock recovery phase locked loop circuits incorporate a counter that detects when no receive signal transitions occur over a significant number of bit intervals which form a loss of signal threshold. Upon detection of loss of signal, the phase locked loop may be forced to retrain to the reference.

Brief Summary Text (9):
There may also be transient disturbances on the receive signal path, however, that result in low transition density for a period of time sufficient to allow a phase locked loop to drift, while not violating a simple loss of signal threshold. To address this situation, many clock recovery phase locked loop circuits incorporate logic to monitor the received data stream and detect when unacceptably low transition density events occur and force retraining to the reference. For example, a clock recovery phase locked loop circuit could have logic that declares loss of signal after 80 bit intervals with no transitions and logic that declares low transition density if there are fewer than 8 transitions in a window of 240 bits, and triggers retraining if either event occurs.

Brief Summary Text (10):
While such a circuit may be fairly simple, it suffers from several drawbacks. Firstly, it may be difficult to prove that such an algorithm will detect all low transition density events that are capable of allowing the phase locked loop to drift sufficiently to lead to the false locking problem. Secondly, if a pessimistic algorithm is chosen so as to have higher confidence of detecting all problematic low transition density events, then the performance of the clock recovery phase locked loop will be downgraded by triggering retraining in many cases where retraining is unnecessary. This will result in a loss of synchronization to the received data stream which is typically plesiochronous to the reference.

Brief Summary Text (13):
Fundamentally, with such attempts to detect problematic transition density events by examining the incoming data stream, one must implement very complex algorithms or accept significant degradation of the potential performance of the clock recovery phase locked loop in order to have high probability of avoiding the false locking problem.

Brief Summary Text (14):
Finally, there may be situations in which transient disturbances on the receive signal path result in high transition densities but nevertheless allow the clock recovery phase locked loop to drift sufficiently to allow false locking to occur. A typical scenario involves use of simple fiber optic receivers that are optimized for long reach. Such receivers of necessity incorporate automatic gain control so as to detect the lowest incoming light levels possible and may have no squelching circuitry so as to extract the maximum in low light level performance.

Brief Summary Text (15):
Under open fiber situations, however, such receive optics typically will generate essentially noise on their outputs, most likely at frequencies related to system noise on the power supply used by the optical receiver. When the output of such optics are fed to a clock recovery phase locked loop that depends on training to a reference as described, under an open fiber condition the phase locked loop may be driven significantly away from its nominal operating frequency with the result that it will not lock when a proper receive signal is restored, hence leading to the false locking problem.

Brief Summary Text (16):
A clock recovery phase locked loop sometimes reverts to an open loop mode, which is undesirable. Clock recovery is typically used at the receiving end of serial data links within systems. In order to minimize the number of circuits connected, high signal bit rates are typically used. In order to minimize cost, it is desirable to use VLSI device implementation technology of the minimum possible frequency capability that can achieve the required performance.

Brief Summary Text (18):
Further, in order to close the control loop around the clock recovery phase locked loop under all conditions, some logic circuitry, typically a divider, must operate at a frequency higher than the upper end of the VCO control range. This puts an onerous constraint on the design of phase locked loop control logic. For example, given typical VCO frequency ranges, when designing a 155 Mbit/s clock recovery circuit, the logic closing the loop must operate above 200 MHz. Similarly, the logic closing the loop for a 622 MHz clock recovery circuit must operate above 800 MHz.

Brief Summary Text (20):
In accordance with the present invention, a clock recovery method and system are realized which ensures that it can never be fooled into a "false locking" mode, and always lock into a legal (e.g. .+-.20 ppm from nominal) signal when it is applied, regardless of the type of signal (loss of signal or noise) that was applied prior to the legal signal. This is effected by forcing the VCO of the phase locked loop to lock to a reference signal source if it is not locked to the legal signal.

Brief Summary Text (21):
The present invention also ensures that the VCO of the phase locked loop is initialized at reset to a frequency below its nominal operating frequency, and be trained in an increasing frequency direction from lowest to nominal operating frequency. This avoids ever having to depend on the VCO and its associated phase locked loop closing circuitry operating at the top end of the frequency range of the VCO.

Brief Summary Text (22):
In accordance with an embodiment of the invention, a method of generating output clock pulses using a phase locked loop which includes a voltage controlled oscillator (VCO) is comprised of the steps (a) providing a sequence of data pulses and a sequence of reference clock pulses, (b) resetting the phase locked loop to force the VCO to its lowest operating frequency, (c) releasing reset of the phase locked loop and forcing the VCO to lock to a multiple of the frequency of the reference clock pulses, (d) detecting the presence of data pulse transitions, (e) in the event of detection of data pulse transitions, forcing the VCO to lock to the data pulses, and (f) outputting output clock pulses from the phase locked loop.

Detailed Description Text (3):
The basic phase locked loop is comprised of a voltage controlled oscillator (VCO) 1, the output of which is applied to the input of a mode divider 3, the output of which is connected to the input of a phase detector 5, the output of which is connected to the input of the VCO through a loop filter 7. The output of the phase detector is connected to the loop filter through a multiplexer, to be described in more detail below. An input data signal RSD (referred to below as the input data signal) from which the clock is to be recovered is applied to another input of phase detector 5.

Detailed Description Text (8):
Recovered clock and data signals RSCLK and RSDO from the phase locked loop are output from the phase detector 5 in a well known manner, e.g. by sampling the serial data stream in the center of its eye and generating phase aligned clock and retimed data outputs RSCLK and RSDO.

Detailed Description Text (9):
General operation of the above circuit is well known. The phase detector 5 detects phase difference between the divided output signal from the VCO and the input data signal, and provides up or down pulses, carried through filter 7, to the VCO, which adjusts its phase or frequency until no further up or down pulses are generated. This basic phase locked loop would suffer from the false locking problem described earlier.

Detailed Description Text (24):
In a successful prototype, after the analog VCO voltage stabilized as determined by the charge pump average current and loop filter components, at least two integration periods were required to enter the "Locked to Data" state. These integration periods are summarized in the following table:

CLAIMS:

1. A method of generating output clock pulses using a phase locked loop which includes a voltage controlled oscillator (VCO) comprising:

(a) providing a sequence of data pulses and a sequence of reference clock pulses,

(b) resetting the phase locked loop to force the VCO to its lowest operating frequency,

(c) releasing reset of the phase locked loop and forcing the VCO to lock to a multiple of the frequency of the reference clock pulses,

(d) detecting the presence of data pulse transitions,

(e) in the event of detection of data pulse transitions, forcing the VCO to lock to the data pulses, and

(f) outputting output clock pulses from the phase locked loop.

7. Apparatus for generating output clock pulses using a phase locked loop which includes a voltage controlled oscillator (VCO) comprising:

(a) means for providing a sequence of data pulses and a sequence of reference clock pulses,

(b) means for resetting the phase locked loop to force the VCO to its lowest operating frequency,

(c) means for releasing reset of the phase locked loop and forcing the VCO to lock to a multiple of the frequency of the reference clock pulses,

(d) means for detecting the presence of transitions of the data pulses,

(e) means for forcing the VCO to lock to the data pulses in the event of detection of data pulse transitions, and

(f) means for outputting output clock pulses from the phase locked loop.

13. A clock recovery circuit comprising:

(a) a digital phase locked loop including, in series, a voltage controlled oscillator, a mode divider connected to the output of the oscillator, a first phase detector connected to the output of the mode divider and a loop filter for receiving an output signal of the phase detector and providing an output signal to the oscillator,

(b) means for applying a digital input signal to another input of the phase detector, whereby the phase detector provides an output signal representing the phase difference between the digital input signal and an output signal of the mode divider,

(c) a reference clock signal input,

(d) a second phase detector for receiving the reference clock signal at an input thereof,

(e) a reference divider for receiving an output signal of the oscillator and for generating a DCLK signal,

(f) means for applying the DCLK signal to another input of the second phase detector,

(g) a clock difference detector for receiving the DCLK signal, the reference clock

signal and an output signal of the mode divider and for generating an out-of-range signal in the event the DCLK and reference clock signals differ by a predetermined number of pulses from the output of the mode divider,

(h) a multiplexer for passing an output signal of either of the phase detectors to the loop filter,

(i) a state machine for receiving the out-of-range signal and for controlling the multiplexer to pass the output signal of the second phase detector to the loop filter in the event of the presence of an out-of-range signal, and to pass the output signal of the first phase detector to the loop filter in the absence of the out-of-range signal.

L7: Entry 32 of 39 File: USPT Sep 3, 1996

DOCUMENT-IDENTIFIER: US 5552733 A
TITLE: Precise and agile timing signal generator based on a retriggered oscillator

Abstract Text (1):
A timing signal generator produces a timing signal having one or more pulses of adjustable phase relative to pulses of a stable reference clock. The timing signal generator employs a low jitter retriggerable oscillator to produce a set of tap signals. The tap signals are frequency locked to the reference clock signal but are evenly distributed in phase. The timing signal generator times the pulses of its output timing signal using pulses of the various tap signals as timing references. Each cycle of the oscillator is triggered by a pulse of the reference clock signal to minimize timing signal jitter. Phase lock loops frequency lock the tap signals to the reference clock and ensure predictability of the timing signal pulse timing relative to the reference clock signal.

Brief Summary Text (7):
Since the propagation delay D of inverters S1-SN is a function of the power supply voltage VPLL supplied in common to all the inverters S1-SN, the frequency of signals T1-TN (1.backslash.2ND) can be controlled by adjusting the voltage of VPLL. A reference oscillator 18 produces an output clock signal (CLOCK) supplied as input to a phase lock controller 20. A delay circuit 22 delays tap signal T1 to provide a second input T1X to phase lock controller 20. Controller 20 includes a phase detector 20A comprising CLOCK to T1X and driving a charge pump 20B charging a capacitor 20C to produce the VPLL signal controlling the frequency of tap signals T1-TN. When CLOCK leads T1X, controller 20 increases the voltage of VPLL to increase the frequency of tap signals TA(1)-TA(N). When CLOCK lags T1X, controller 20 decreases the voltage of VPLL to decrease tap T1-TN signal frequency. Thus controller 20 phase locks signal T1X to CLOCK. Since T1X is derived from T1, all tap signals TA(1)-TA(N) are frequency locked to CLOCK.

Brief Summary Text (14):
In accordance with another aspect of the invention, the timing signal generator includes a circuit for synthesizing the timing signal using the tap signals as time references for controlling timing of pulses in the timing signal. The timing signal synthesizer also produces a clock signal CLOCK3 having the same frequency as the TA(1) tap signal but which is delayed from TA(1) by the delay inherent in the signal processing path between the tap signals and the timing signal. A first phase lock loop controller compares CLOCK3 to a similarly delayed CLOCK1 signal and adjusts the RVCO oscillation rate to bring TA(1) into phase with CLOCK1, thereby stabilizing the timing of the tap signal pulses and establishing a predictable phase relationships between CLOCK1 signals and the timing signal pulses.

Brief Summary Text (15):
In accordance with a further aspect of the invention, the timing signal path within the timing signal processor includes a delay circuit having a delay that is dynamically adjusted by a second phase lock loop controller. The second phase lock loop controller compares the CLOCK1 signal to the TA(1) signal and adjusts the delay of the delay circuit so as to phase lock TA(1) to the CLOCK1 signal. This adjustment cancels out any changes in the delay inherent in timing signal path that may be due to temperature or process variations that would otherwise affect the timing signal and the CLOCK1 signal.

Drawing Description Text (12):
FIG. 9 illustrates in block diagram form the phase lock loop controller of FIG. 2A that produces the VX signal.

Detailed Description Text (3):
Timing signal generator 30 includes a retriggerable, voltage controlled oscillator (RVCO) 36, a signal synthesizer 38, an RVCO controller circuit 40, and a reference delay circuit 49. RVCO 36 receives the CLOCK1 signal from ROSC 33 and a phase lock loop control signal (VPLL) from RVCO controller 40 and produces a set of N periodic output tap signals TA(1)-TA(N). RVCO controller 40 is a conventional phase lock loop controller for producing an output signal VPLL proportional to the integral of the phase difference between its input signals CLOCK4 and CLOCK3. The reference delay circuit 49 delays the CLOCK1 signal to produce CLOCK4. The signal synthesizer 38 synthesizes the CLOCK3 signal using the TA(1)-TA(N) signals as timing references. CLOCK3 has the same frequency as the TA(1) tap signal but is delayed from TA(1) by the same delay as CLOCK4 is delayed from CLOCK1. Controller 40 controls the level of VPLL so as to phase lock CLOCK3 to CLOCK4. Since CLOCK3 is phase shifted from TA(1) by the same amount as CLOCK4 is phase shifted from TA(1), the VPLL signal also phase locks the TA(1) signal to CLOCK1.

Detailed Description Text (5):
Synthesizer 38 includes a first on-the-fly selector 41 for producing a second clock signal (CLOCK2) of a desired adjustable frequency (e.g. 25-50 MHz) by selecting pulse edges of various TA(1)-TA(N) signals to control the timing of pulse edges of the CLOCK2 signal. The CLOCK2 signal passes into an adjustable delay circuit 42 to produce a delayed clock signal CLOCK2'. A phase lock loop controller 43 adjusts the delay of circuit 42. (The purpose of this adjustable delay is discussed herein below.) The CLOCK2' signal passes into a phase splitting delay circuit 44 producing a second set of tap signals TB(1)-TB(2N). The TB(1)-TB(2N) signals have the same frequency as the CLOCK2' signal but their phases are evenly distributed. The TB(1)-TB(2N) signals are supplied to another on-the-fly selector 46 synthesizing the desired TIMING signal using one or more of the TB(1)-TB(2N) signals as a timing references.

Detailed Description Text (7):
FIG. 2B is a block diagram illustrating time delays associated with the timing signal generator of FIG. 2A. Referring to FIGS. 2A and 2B, the signal path delay through selector 41 is represented as DELAY1. The signal path delays of circuits 42, 43, 46, 48 and 49 are represented as delays DELAY2, DELAY3, DELAY4A, DELAY4B and DELAY5, respectively. The values of DELAY1, DELAY3, DELAY4A and DELAY4B and DELAY5 vary in inverse relation to the voltage of the VPLL signal produced by RVCO controller 40. The value of DELAY2, the delay provided by adjustable delay circuit 42, varies inversely with the VX signal produced by phase lock loop controller 43 of FIG. 2A. The signal paths through selectors 46 and 48 are similar and therefore DELAY4A and DELAY4B are equal. Thus the processing delay of the "timing signal path" through devices 41, 42, 44 and 46 will be equal to the "reference signal path" through devices 41, 42, 44 and 48.

Detailed Description Text (8):
As mentioned above reference delay circuit 49 is designed so that DELAY5 is equal to the sum of the nominal values of DELAY1, DELAY2, DELAY3, and DELAY4A (or DELAY4B). The devices that produce these delays are made up of transistor gates having signal propagation speeds controlled by their power supplies. The VPLL signal supplies power to all gates in the timing signal path except those forming adjustable delay circuit 42. These gates obtain their power supply VX from controller 43. The reference delay circuit 49 is suitably a series of inverter gates that the CLOCK1 signal must pass through to become the CLOCK4 signal. Each inverter gate in the series corresponds to, and is similar in construction to, a separate gate in the timing (or reference) signal path through devices 41, 42, 44 and 46 (or 48). If the VX signal voltage were equal to the VPLL signal voltage we might expect the reference path delay through circuit 49 to match the timing signal path delay through devices 41, 42, 44 and 46 (or 48) since each path has the same number and type of gates and since they all would have the same power supply voltage level. However due to temperature and process variations between the various components, the actual signal propagation rate in gates forming devices 41, 42, 44 or 46 (or 48) may differ from the propagation rate of corresponding gates forming the reference delay circuit 49. Without compensating for such differences, the delay (DELAY5) through reference delay circuit 49 would not match the timing or reference signal

path delay through devices 41, 42, 44 and 46 (or 48). In such event, TA(1) would not be in phase with the CLOCK1 signal and TIMING signal pulses would not occur at the expected times.

Detailed Description Text (10):
Thus the timing signal generator 30 of FIG. 2A involves two phase lock loops. Both loops seek to phase lock the TA(1) signal to the CLOCK1 signal. The "primary" loop involving controller 40 indirectly monitors the phase difference between CLOCK1 and TA(1) (by monitoring CLOCK4 and CLOCK3) and directly adjusts the phase of TA(1) relative to CLOCK1 by adjusting VPLL. The "secondary" loop involving controller 43 directly monitors the phase relationship between CLOCK1 and TA(1) and indirectly adjusts their phase relationship by adjusting the timing signal path delay. The two phase lock loops work together to minimize tap signal jitter.

Detailed Description Text (12):
Delay circuit 51 functions as a phase distribution circuit, generating a succession of signal pulses in response to each pulse of a trigger signal (TRIG) from trigger circuit 50. The successive pulses are shifted in time by regular intervals and each pulse is conveyed by a separate output tap signal TA(1)-TA(N). The TA(1)-TA(N) tap signals appear at the inputs of stages I1-IN. The phase shift interval between pulses is equal to the signal propagation delay of stages I1-IN. Stages I1-IN all have the same signal propagation delay, a function of the VPLL signal forming the power supply to each oscillator stage I1-IN.

Detailed Description Text (16):
Referring to FIG. 5 illustrating the phase splitting delay circuit 44 of FIG. 2A in block diagram form, delay circuit 44 comprises a set of inverter stages V(1) though V(2N-1) connected in series. The first stage V(1) receives the CLOCK2' signal, which also servers as the TB(1) tap signal. The remaining TB(2)-TB(2N) tap signals are taken at outputs of stages V(1)-V(2N-1). The stages of delay circuit 44 are identical to the stages of delay circuit 51 of RVCO 36 of FIG. 3A and they are controlled by the power supply signal VPLL. Thus the delay of each stage of delay circuit 44 of FIG. 5 is the same as the stage delay of circuit 51, and the phase difference between tap signals TB(1)-TB(2N) is 1/Nth of one cycle of the CLOCK1 signal. Since the period of CLOCK2' may be twice as long as the period of CLOCK1, delay circuit 44 needs to produce twice as many tap signals as oscillator 36 in order to divide the CLOCK2' signal with the same resolution as the TA(1)-TA(N) signals divide the CLOCK1 signal. When the CLOCK2' signal has a period that is less than twice that of CLOCK1, some of the TB(1)-TB(2N) signal inputs to selector 46 are redundant.

Detailed Description Text (22):
FIG. 9 illustrates phase lock loop controller 43 of FIG. 2A. A phase comparator 80 charges or discharges a capacitor 82 in proportion to the phase difference between CLOCK1 and TA(1). An amplifier 84 amplifies voltage across capacitor 82 to produce the VX signal.

Detailed Description Text (23):
Thus has been described a timing signal generator employing a retriggerable voltage controlled oscillator to produce a set of tap signals used to control the timing of pulses of an output timing signal with high resolution and predictability. The signal generator uses phase lock loops to control the oscillator so that signal timing is predictable and stable. While the forgoing specification has described preferred embodiment(s) of the present invention, one skilled in the art may make many modifications to the preferred embodiment without departing form the invention in its broader aspects. The appended claims therefore are intended to cover all such modifications as fall within the true scope and spirit of the invention.

L7: Entry 3 of 39 File: USPT Jul 23, 2002

DOCUMENT-IDENTIFIER: US 6424230 B1
TITLE: Loop stabilization technique in a phase locked loop (PLL) with amplitude compensation

Abstract Text (1):
A phase locked loop circuit and method that substantially decouples control of the phase/frequency and the amplitude of the oscillation output such that the frequency of the oscillation can be controlled independently of the amplitude. The phase locked loop circuit comprises a phase/frequency control loop and an amplitude control loop wherein both loops control an oscillator that oscillates at a certain frequency in response to a phase/frequency control signal generated by the phase/frequency control loop. In addition, the oscillation amplitude is determined by an amplitude control signal generated by the amplitude control loop. As with conventional circuits of this type, a parasitic gain is coupled from the amplitude control loop into the phase/frequency control loop, thereby causing interference between the loops that leads to stability problems. To counter the coupling of the parasitic gain, an inverted gain is inserted from the amplitude control loop into the phase/frequency control loop in opposite to the parasitic gain, so as to effectively cancel the interference. The circuit and method also provide for canceling the opposite parasitic gain that is coupled from the phase/frequency loop into the amplitude control loop.

Brief Summary Text (3):
The present invention generally concerns the control of a phase locked loop (PLL), and in more particular concerns the simultaneous control of frequency and amplitude in a PLL.

Brief Summary Text (5):
Amplitude control of an oscillator over process, temperature, and power supply variations is a challenging task in PLL design. Uncontrolled oscillation amplitude can be a source of additional jitter due to changing operating points and cyclostationary device noises. Another application that requires amplitude control in PLLs is the master-slave tuning in on-chip filters. Oscillation amplitude of the PLL should match with the signal amplitude processed in the filter to avoid distortion that causes frequency errors. However, active amplitude compensation incorporated into a PLL can be a major problem of stability. Consider a gm-C (transconductance-Cell) based relaxation type oscillator. The loop introduced to control amplitude interferes with the main phase/frequency locking loop. The mechanism that adjusts the amplitude, i.e., the current of the negative gm load of the oscillator where the negative gm load is used to compensate for resistive losses, initiates the oscillation cycle as well as sets the oscillation amplitude, thereby imposing an inverse force that causes the two loops that fight each other, wherein precise control of one of the loops has an adverse effect on the control of the other loop. The traditional solution to minimize the problem is to maximize the difference between time constants governing the amplitude and phase/frequency locking loops. Basically, the amplitude loop should be slowed down by using large component values, such as huge capacitors, which consumes more area and power than desired. Still, the system should be overdesigned to have enough margin to accommodate not only the environmental variables, but also component values especially for large time constants.

Drawing Description Text (3):
FIG. 1 is a schematic block diagram of a conventional charge pump PLL with amplitude control;

Drawing Description Text (8):
FIG. 6 is a schematic block diagram for modeling the behavior of the conventional charge pump PLL of FIG. 1;

Drawing Description Text (9):
FIG. 7 is a schematic block diagram for modeling the behavior of a modified charge pump PLL circuit in accord with a first exemplary implementation of the present invention; and

Drawing Description Text (10):
FIG. 8 is a schematic block diagram for modeling the behavior of a modified charge pump PLL circuit in accord with a second exemplary implementation of the present invention.

Detailed Description Text (2):
A conventional charge pump based PLL system 10 that includes amplitude control is depicted in FIG. 1. PLL system 10 comprises an amplitude control loop 12 and a phase/frequency control loop 14 that provide a pair of input signals to a current-controlled oscillator (ICO) 16 that is common to both control loops. As will be understood by those skilled in the art, although two separate lines corresponding to an amplitude output signal 17 (A.sub.out) and a frequency output signal 18 (F.sub.out) are shown in FIG. 1, A.sub.out and F.sub.out represent components of a single composite signal that is output by ICO 16. Amplitude control loop 12 includes a peak detector/comparator 19, an amplitude loop filter 20, a voltage-to-current converter 22, and current-controlled oscillator (ICO) 16. Phase/frequency control loop 14 includes a phase detector 24, a charge pump 26, a frequency loop filter 28, a voltage-to-current converter 30, ICO 16, and an optional frequency divider 32. If frequency divider 32 is used, frequency output signal 18 becomes frequency output signal 18' after its frequency is divided.

Detailed Description Text (4):
Phase/frequency control loop 14 works in a similar manner. The loop receives a frequency reference input signal 44 that is compared with frequency output signal 18' in phase detector 24. Phase detector 24 outputs a pair of control signals 48 and 50 that are fed into charge pump 26, which pumps a current 52 that is proportional to the phase difference between signal 44 and 18'. Then current 52 is filtered by phase/frequency loop filter 28 through means of passive elements C.sub.2, C.sub.3, and R.sub.2 to produce a frequency control voltage 54. Frequency control voltage 54 is then fed into voltage-to-current converter 30, which outputs a frequency control current signal 56 that drives ICO 16.

CLAIMS:

1. A method for stabilizing a phase/frequency control loop in the presence of an amplitude control loop in a phase locked loop circuit, comprising: determining a first parasitic gain that is coupled from the amplitude control loop into the phase/frequency control loop; and inserting a first inverse gain into the phase/frequency control loop that is substantially equal to the first parasitic gain and opposite thereto to cancel the effect of the first parasitic gain by summing a scaled amount of an amplitude control current used to control the amplitude control loop into a phase/frequency control current used to control the phase/frequency control loop.

2. The method of claim 1, wherein the phase locked loop circuit includes a gm (transconductance)-C relaxation-type oscillator that is common to both of the phase/frequency and amplitude control loops.

4. The method of claim 3, wherein the phase locked loop circuit has an oscillation cycle and produces an oscillation having an amplitude, and wherein each gm stage is loaded with a net negative gm circuit that produces a net negative amount of transconductance at its output to compensate for resistive losses, initiate the oscillation cycle, and set the oscillation amplitude.

9. A phase locked loop circuit comprising: a phase/frequency control loop including a gm (transconductance)-C relaxation-type oscillator that produces an output signal

having a frequency corresponding to a frequency control signal; an amplitude control loop including the gm-C relaxation-type oscillator such that the output signal has an amplitude corresponding to an amplitude control signal, said amplitude control loop coupling a parasitic gain into the phase/frequency control loop and providing an inverted gain in opposite to the parasitic gain to the phase/frequency control loop to substantially cancel the effect of the parasitic gain such that control of the phase/frequency of the phased locked loop circuit is decoupled from control of the amplitude of the phase locked loop circuit.

10. The phase locked loop circuit of claim 9, wherein the gm-C relaxation-type oscillator comprises two cascaded gm stages that provide 180 degrees of phase shift.

11. The phase locked loop circuit of claim 9, wherein the phase locked loop circuit has an oscillation cycle and produces an oscillation having an amplitude, and wherein each gm stage is loaded with a net negative gm circuit that produces a net negative amount of transconductance at its output to compensate for resistive losses, initiate the oscillation cycle, and set the oscillation amplitude.

12. The phase locked loop circuit of claim 11, wherein each net negative gm circuit comprises m source-coupled cross-connected differential pairs with resistive loads in parallel with n source coupled diode-connected differential pairs with resistive loads, wherein m>n.

13. The phase locked loop circuit of claim 12, wherein the resistive loads are produced by saturated PMOS transistors.

14. A phase locked loop circuit comprising: a phase/frequency control loop including: a phase detector; an integrator; a first loop filter; a first voltage to current converter; and a current-controlled oscillator; and an amplitude control loop including: a peak detector/comparator; a second loop filter; a second voltage-to-current converter; and the current-controlled oscillator, wherein a parasitic gain is coupled from the amplitude control loop into the phase/frequency control loop and an inverted gain is inserted into the phase/frequency control loop opposite to the parasitic gain to substantially cancel the effect of the parasitic gain such that control of the phase/frequency control loop is decoupled from the amplitude control loop.

L2: Entry 6 of 19 File: USPT May 9, 1995

DOCUMENT-IDENTIFIER: US 5414390 A
TITLE: Center frequency controlled phase locked loop system

Detailed Description Text (5):
The operation of current copier 80 utilizing sample and hold circuit 82 is shown in greater detail in FIG. 3. FET 90 in voltage to current converter VCO2 74 controls the current controlled oscillator ICO2 76. The voltage V.sub.b on the gate of FET 90 is mirrored at the gate of FET 92 in copier 80 to create an identical current, here called I.sub.CF to drive current to voltage converter 72. Since both current to voltage converters 76 and 72 are identical in terms of their process and fabrication, the same current applied to both will cause both circuits to provide the same output frequency within a few percent. When it is desired to read the associated disk, a read gate signal opens switch 94 in sample and hold circuit 82 so that capacitor C 96 stores the voltage then present and maintains that voltage on the gate of FET 92 during the entire read operation, so that it is only the frequency of the read signal which is affecting the frequency of the phase locked loop system.

DOCUMENT-IDENTIFIER: US 5422911 A
TITLE: Frequency walled phase lock loop

Brief Summary Text (11):
a programmable gain current multiplier coupled to the voltage to current converter, a gain of the programmable gain current multiplier being determined at least in part by a control word selected such that a loop gain of the phase lock loop frequency synthesizer remains relatively constant over a predetermined operating domain of the programmable output frequency signal, the programmable gain current multiplier operating to generate a control current signal by subtracting a reference current from a limited current, thus bounding a range of the control current signal within a maximum value of substantially the reference current and a minimum value of the difference between the reference current and the limited current;

Detailed Description Text (20):
The output current 416 from the voltage to current converter 410 is subtracted from a current 415 generated by a current reference 411 to generate a control current 417 that sets the output frequency of a current controlled oscillator 413. The voltage to current converter 410 output current is set to a maximum value of 50% of the reference current. This provides a restricted current swing (restricted domain) to obtain the walled operation, thus allowing the frequency of the current controlled oscillator 413 to vary only within the bounds of the voltage to current converter 410 output current. This operation inherently improves phase lock loop performance by limiting the maximum frequency excursion, thus allowing for faster frequency lock times.

Detailed Description Text (22):
A selective call receiver comprising a receiver 103 for providing a received signal; a demodulator 104 for recovering the received signal and providing an information signal; a decoder 105 for correlating a recovered address contained within the information signal with a predetermined address corresponding to the selective call receiver, and responsive to said addresses substantially correlating, generating a PG,11 detection indicating selection of the selective call receiver; and a support circuit 108 to process information for presentation in response to the detection, embodies the preferred environment for implementing the phase lock loop frequency synthesizer. In this case, the a phase lock loop frequency synthesizer, having a programmable output frequency signal usable by at least the receiver 103, the decoder 105, and the support circuit 108, comprises: a charge pump phase/frequency detector 403, 408 having a detector output signal representing a phase/frequency difference between a reference frequency signal 402 and the programmable output frequency signal 414; a voltage to current converter 410 coupled to the charge pump phase/frequency detector for converting a band-limited spectra of a filter output voltage to a limited current representing the phase/frequency difference between the reference frequency signal 402 and the programmable output frequency signal 414; a programmable gain current multiplier 412 coupled to the voltage to current converter, a gain of the programmable gain current multiplier being determined at least in part by a control word selected such that a loop gain of the phase lock loop frequency synthesizer remains relatively constant over a predetermined operating domain of the programmable output frequency signal 414, the programmable gain current multiplier 412 operating to generate a control current signal 417 by subtracting a reference current 415 from a limited current 416, thus bounding a range of the control current signal within a maximum value of substantially the reference current 415 and a minimum value of the difference between the reference current 415 and the limited current 416; a current controlled variable frequency oscillator 413 coupled to the programmable gain current multiplier 412, the current

controlled variable frequency oscillator producing the programmable output frequency signal 414 in response to the control current signal 417; and a programmable frequency divider 405 coupled to the current controlled variable frequency oscillator 413 and a charge pump phase/frequency detector 403, the programmable frequency divider division ratio and scaled output feedback frequency 404 being determined by the control word.

CLAIMS:

1. A phase lock loop frequency synthesizer having a scalable output frequency signal, the phase lock loop frequency synthesizer comprising:

a charge pump phase/frequency detector having a detector output signal representing a phase/frequency different between a reference frequency signal and the scalable output frequency signal;

a voltage to current converter coupled to the charge pump phase/frequency detector for converting a band-limited spectrum to a limited current representing the phase/frequency difference between the reference frequency signal and the scalable output frequency signal;

a programmable gain current multiplier coupled to the voltage to current converter, a gain of the programmable gain current multiplier being determined at least in part by a control word selected such that a loop gain of the phase lock loop frequency synthesizer remains relatively constant over a predetermined operating domain of the scalable output frequency signal, the programmable gain current multiplier operating to generate a control current signal by subtracting a reference current from a limited current, thus bounding a range of the control current signal within a maximum value of substantially the reference current and a minimum value of the difference between the reference current and the maximum value of the limited current;

a current controlled variable frequency oscillator coupled to the programmable gain current multiplier, the current controlled variable frequency oscillator producing the scalable output frequency signal in response to the control current signal; and

a programmable frequently divider coupled to the current controlled variable frequency oscillator and a charge pump phase/frequency detector, the programmable frequency divider division ratio and scaled output feedback frequency being determined by the control word.

4. A selective call receiver, comprising;

a receiver for providing a received signal;

a demodulator for recovering the received signal and providing an information signal;

a detector for correlating a recovered address contained within the information signal with a predetermined address corresponding to the selective call receiver, and responsive to said addresses substantially correlating, generating a detection signal indicating selection of the selective call receiver;

a support circuit to process information for presentation in response to the detection signal; and

a phase lock loop frequency synthesizer having a scalable output frequency signal usable by at least the receiver, the decoder, and the support circuit, the phase lock loop frequency synthesizer comprising:

a charge pump phase/frequency detector having a detector output signal representing a phase/frequency difference between a reference frequency signal and the scalable output frequency signal;

a voltage to current converter coupled to the charge pump phase/frequency detector

for converting a band-limited spectrum to a limited current representing the phase/frequency difference between the reference signal and the scalable output frequency signal;

a programmable gain current multiplier coupled to the voltage to current converter, a gain of the programmable gain current multiplier being determined at least in part by a control word selected such that a loop gain of the phase lock loop frequency synthesizer remains relatively constant over a predetermined operating domain of the scalable output frequency signal, the programmable gain current multiplier operating to generate a control current signal by subtracting a reference current from a limited current, thus bounding a range of the control current signal within a maximum value of substantially the reference current and a minimum value of the difference between the reference current and the maximum value of the limited current;

a current controlled variable frequency oscillator coupled to the programmable gain current multiplier, the current controlled variable frequency oscillator producing the scalable output frequency signal in response to the control current signal; and

a programmable frequency divider coupled to the current controlled variable frequency oscillator and a charge pump phase/frequency detector, the programmable frequency divider division ratio and scaled output feedback frequency being determined by the control word.

L15: Entry 3 of 8 File: USPT Oct 15, 1996

DOCUMENT-IDENTIFIER: US 5566204 A
TITLE: Fast acquisition clock recovery system

Detailed Description Text (3):
Referring more particularly to FIG. 1, the phase-locked loop 16 of transmitter section 12 includes frequency detector 20 having an output fed to a conventional charge pump 26 which may preferably be a differential charge pump. The output of charge pump 26 is coupled to loop filter 28 which includes a capacitor 30 connected to ground. Loop filter 28 is connected to a conventional voltage to current converter 32 that converts the voltage on capacitor 30 to transmitter correction current i.sub.tc that is fed to current adder 34. The other input to current adder 34 is a transmitter reference or bias current i.sub.tb from current source 36 resulting in a transmitter total feedback current i.sub.tt that is fed to current mirror 37 to control current controlled oscillator 18. The output of current controlled oscillator 18 is fed to an optional divide circuit 38 before being coupled to frequency detector 20 to be compared with an external frequency reference. For example, if the external frequency reference is 20 MHz and the divide circuit 38 divides by 10, the transmitter total feedback current i.sub.tt will cause the phase-locked loop 16 to lock when the output of current controlled oscillator is driven to 200 MHz. Simply stated, a conventional phase-locked loop 16 is used to lock the output of current controlled oscillator 18 to a predetermined frequency such as 200 MHz which is subsequently used to transmit data to a remote receiver section 14. It is noted that the operation of phase-locked loop 16 is dependent on the external frequency reference which presumably is always present, so the output of the current controlled oscillator 18 will be continuously held at the predetermined transmission frequency.

Detailed Description Text (6):
The output of XOR 52 is coupled to phase detector 54 that is part of phase-locked-loop (PLL) 22. A phase detector is used instead of a frequency detector because phase detectors are generally faster and do not malfunction when one of the input waveforms has missing transitions. That is, a frequency detector could not generally be used unless the input data signal had continuously alternating states. Phase-locked loop 22 further includes multiplexer 56, charge pump 58, loop filter 60 including capacitor 62, voltage to current converter 64, current adder 66, and current controlled oscillator 24. Multiplexer 56 is controlled by transition detector 68 which detects whether an incoming data signal is being received at terminal 40. More specifically, transition detector 68 operates to control multiplexer 56 to couple the output of phase detector 54 to charge pump 58 during this first mode of operation when an incoming data signal is being received, and to couple the output of frequency detector 70 to charge pump 58 during a second mode of operation when incoming data is not being received. Thus, in the first mode of operation now being described, the output of phase detector 54, and thus charge pump 58, is dependent on the phase relationship between the output of XOR 52 and the output of current controlled oscillator 24. More specifically, according to well known phase-locked loop principles, the average output current of charge pump 58 is zero when the output of current controlled oscillator 24 is synchronized in frequency and phase to the embedded NRZ data frequency component in the output of XOR 52. Under such condition, the charge on capacitor 62, the output receiver correction current i.sub.rc from voltage to current converter 64, and the receiver total feedback current i.sub.rt all remain constant. Thus, the output frequency of current controlled oscillator 24 remains the same.

Detailed Description Text (7):
In contrast, when there is a phase difference between the output of current

controlled oscillator 24 and the originating clock embedded in the output of XOR 52, an error signal from phase detector 54 causes charge pump 58 to charge or discharge capacitor 62 to provide a change in receiver correction current i.sub.rc from voltage to current converter 64 that functions to adjust current controlled oscillator 24 into synchronism with the frequency component of the originating clock for the incoming NRZ data. The receiver correction current i.sub.rc from voltage to current converter 64 is added with a receiver bias current i.sub.rb that is substantially equal to the transmitter total current i.sub.tt used to control the transmitter current controlled oscillator 18. Thus, an error signal from phase detector 54 increases or decreases to increase or decrease the frequency of current controlled oscillator 24 to drive its output into frequency and phase synchronism with the originating clock embedded in the output of XOR 52. For example, if the originating clock of the incoming NRZ data is at a 200 MHz rate, phase-locked loop 22 will lock when the output of current controlled oscillator 24 is at a 200 MHz rate, and the transitions are aligned as shown in FIG. 2D. However, as can be seen by comparing FIG. 2D with the incoming NRZ data in FIG. 2A, the output from current controlled oscillator 24 that is used in the phase-locked loop 22 to feed phase detector 54 is not properly aligned to function as the clock for decision circuit 44. More specifically, the positive transitions of the clock from current controlled oscillator 24 are aligned to catch the NRZ data at point A as shown in FIG. 2A rather than at the optimum position B in the middle of the bit period. Thus, it is desirable to provide a clock that is in quadrature, or has a shift in phase of 90.degree. from the output of current controlled oscillator 24 that is fed to phase detector 54. The phase shift function is provided by 90.degree. delay 72 which delivers to decision circuit 44 the quadrature waveform as shown in FIG. 2E. In response to the positive transitions in the example waveform of FIG. 2E, decision circuit 44 catches the NRZ data at point B in the middle of the bit periods.

Detailed Description Text (10):
The coarse step is implemented by using the transmitter total feedback current it in the transmitter phase-locked loop 16 to control the free running operation of the current controlled oscillator 24. More specifically, with reference still to FIG. 1, current mirror 37 causes the receiver bias current added i.sub.rb to current adder 66 to be substantially equal to transmitter total feedback current i.sub.tt that is used to control current controlled oscillator 18. Thus, assuming the receiver correction current i.sub.rc from voltage to current converter 64 to be relatively small, the free running or receiver bias current i.sub.rb provided to receiver current controlled oscillator 24 through current adder 66 will approximate the total feedback current i.sub.tt used to control transmitter current controlled oscillator 18. Because the two current controlled oscillators 18 and 24 are on the same integrated circuit and are fairly well matched, the free running frequency of the receiver current controlled oscillator 24 will be near to the operating frequency of the transmitter current controlled oscillator 18. For example, if current controlled oscillator 18 is operating at 200 MHz, current controlled oscillator 24 will also operate at approximately 200 MHz.

Current US Cross Reference Classification (8):
375/376

CLAIMS:

16. The system recited in claim 15 wherein said locked loop of said transmitter further comprises a charge pump, a loop filter, and a voltage to current converter wherein said charge pump is responsive to said transmitter frequency detector, said loop filter is responsive to said charge pump, said voltage to current converter is responsive to said loop filter, and said transmitter current adder is responsive to said voltage to current converter.

17. The system recited in claim 15 wherein said first and second locked loops of said receiver further comprise a charge pump, a loop filter, and a voltage to current converter wherein said charge pump is responsive to said multiplexer, said loop filter is responsive to said charge pump, said voltage to current converter is responsive to said loop filter, and said receiver current adder is responsive to said voltage to current converter.

18. On a transmitter and receiver integrated circuit adapted for receiving and transmitting data signals, said integrated circuit comprising:

a transmitter section comprising a phase-locked loop comprising a first frequency detector, a charge pump, a loop filter, a voltage to current converter, a current adder, and a current controlled oscillator connected in a loop, said frequency detector being responsive to an output of said current controlled oscillator and a reference clock to lock said current controlled oscillator output to a predetermined frequency; and

a receiver section comprising a 90.degree. delay adapted to receive an incoming non-return-to-zero data signal and provide an output signal shifted in phase by 90.degree.;

said receiver section further comprising an exclusive OR responsive to said incoming data signal and said phase shifted signal for providing an output signal having a frequency component of an originating clock of said non-return-to-zero incoming data signal;

said receiver section further comprising a transition detector responsive to said incoming data signal for providing a control signal indicating the presence or absence of an incoming data signal;

said receiver section further comprising first and second phase-locked loops each in common comprising a multiplexer, a charge pump, a loop filter a voltage to current converter, a current adder and a current controlled oscillator connected in series, said first phase-locked loop further comprising a second frequency detector connected between said receiver current controlled oscillator and said multiplexer, said second phase-locked loop further comprising a phase detector connected between said receiver current controlled oscillator and said multiplexer;

said multiplexer being responsive to said transition detector to select said second frequency detector as its input to activate said first phase-locked loop during a first mode of operation in the absence of an incoming data signal and to select said receiver phase detector as its input to activate said second phase-locked loop during a second mode of operation in the presence of an incoming data signal;

said second frequency detector further being responsive to said transmitter current controlled oscillator to cause said receiver current controlled oscillator to have an output frequency substantially the same as said transmitter current controlled oscillator during said first mode of operation; and

said receiver phase detector further being responsive to said exclusive OR to cause said receiver current controlled oscillator to have an output frequency substantially the same as an originating clock of said incoming data signal during said second mode of operation.

L8: Entry 22 of 204 File: USPT Jan 20, 1998

DOCUMENT-IDENTIFIER: US 5710526 A
TITLE: Phase-locked loop for signals having rectangular waveforms

YEAR FILED (1):
1996

Abstract Text (1):
Phase-locked loop (for signals having rectangular waveforms, comprising, in series, a phase detector, a control signal generator circuit having a loop filter, a controlled oscillator and an auxiliary circuit. The detector recieves a reference signal having a reference frequency from a reference source as first input signal. The detector recieves second and third input signals from the auxiliary circuit. The reference signal and the second input signal are compared by a first logic combination function to deliver a second combination signal. The second and third input signals are compared by a second logic combination function to deliver a second combination signal. The second and third input signals are such that, in the locked state of the loop, the frequency of the second input signal is equal to the reference fequency and the frequency of the second combination signal is equal to twice the reference frequency and the duty cycle of the second combination signal differs from the duty cycle of the reference signal. The difference between the two combination signals is delivered to the control signal generator circuit. For a frequency difference between the first and second input signals of the detector, the control signal generator circuit controls the oscillator so as to set the oscillator frequency in a direction towards an extreme oscillator frequency. If the loop does not lock while traversing this path, the control signal generator circuit will adjust the loop and control the oscillator in such a way that the oscillator fequency is set in the opposite direction towards a second extreme frequency. The two extreme oscillator frequencies are chosen below and above the desired oscillator frequency, respectively.

Brief Summary Text (2):
The invention relates to a phase-locked loop.

Brief Summary Text (3):
Such a phase-locked loop is disclosed, for example, in the book entitled "Samenvattingen van de post-academische cursus Phase Lock Loop"("Summaries of the post-academic course entitled Phase Lock Loop"), Delft Technical University, Electronics Department, January 1980, pages 99 to 101 inclusive. In the latter, use is made of a phase detector comprising a single digital multiplier, for example an exclusive OR gate, a NAND gate or an OR gate. The input signals of the detector have a square waveform. The detector has a transfer characteristic f(.theta.), .theta. being the phase difference between the input signals, one of which is a reference signal, of the detector having a cyclic triangular waveform which is completely above f(.theta.)=0, with a minimum at f(0.+-.M 360.degree.), where M is an integer (see FIG. 5 of this application). The loop is so adjusted that in the locked state, that is to say with no frequency difference between the input signals of the detector, .theta.=90.degree., i.e. the two input signals of the detector are shifted by 90.degree. with respect to one another, as a result of which the detector provides, in the locked state ("in-lock"), an output signal having a pulsed form with a frequency which is twice the reference frequency and whose pulse width is equal to 1/4 of the cycle of the reference signal. In the locked state, or quiescent state, of the loop, the detector therefore provides a strongly pulsating output signal, said pulses forming the so-called ripple of the output signal of the detector in the locked state, in which state the control signal has a quiescent level for the oscillator. Because the pulses have a high energy content, they have a

strongly disturbing influence on the frequency stability of the output signal of the oscillator. Because it is a point half way up the slopes of the triangular transfer characteristic of the detector which is the equilibrium point for the locked state of the loop, the output signal of the detector is independent of a frequency difference between the input signals of the detector as seen over a number of cycles of the reference signal, all the phase differences between the input signals of the detector being traversed; or in other words, the averaged output signal of the detector as seen over a number of cycles of the reference signal is independent of a frequency difference between the input signals of the detector. In the case of a frequency difference between the input signals of the detector which is great with respect to the loop bandwidth, the capture will take place slowly or in a creeping manner, which is very undesirable for many applications of the phase-locked loop.

Brief Summary Text (5):
The object of the invention is to improve the known phase-locked loop.

Brief Summary Text (6):
This object is achieved by means of the phase-locked loop according to the present invention. As a result, in the case of a frequency difference between the reference signal and another input signal of the phase detector, the oscillator receives a control signal which rapidly sets the loop to the locked state.

Brief Summary Text (7):
Preferably, the phase-locked loop is constructed to provide a cyclic transfer characteristic f(.theta.) having a triangular waveform for which f(.theta.)=0 in the locked state of the loop. The points of the triangular waveforms occur at an interval of 180.degree. and not at .theta.=0. The equilibrium point of the loop is therefore on a slope at .theta.=0. As a result, no ripple appears, in principle, on the output signal of the detector in the locked state, as a result of which the oscillator is not disturbed by such a ripple and the oscillator delivers a more stable output frequency in the locked state. With imperfect operation of the loop in the locked state, only a small ripple occurs which has a small energy content and double the frequency of the reference frequency, which ripple is easy to remove or to minimize.

Brief Summary Text (11):
Known phase-locked loops, in which a sequential phase detector is used, for example an SPD ("sequential phase detector") or an SFPD ("sequential frequency and phase detector"), which are also described in the above-mentioned book entitled "Samenvattingen van de postacademische cursus Phase Lock Loop", make use of one or more memory elements (flip-flops) in which case, as a result of different delays and different finite switching times of logic elements and as a result of instability of the switching levels of the logic elements of the detector and, consequently, undefined logic state combinations, parasitic ("spurious") signals may occur in the output signal of the detector and which signals disturb the operation of the loop. As a result of the absence of such memory elements in the phase detector of the invention, the disadvantageous effect of such parasitic signals is largely absent. This is despite the fact that the detector according to the invention receives not only the reference signal of the auxiliary circuit, but also two input signals which are time-dependent on one another. The effect of any parasitic signals which may nevertheless occur can readily be suppressed according to the invention.

Drawing Description Text (8):
FIG. 10 shows a more detailed diagram of a first embodiment of a phase-locked loop according to the invention;

Drawing Description Text (11):
FIGS. 13 to 20 inclusive show characteristics illustrating various possible operations of various embodiments of the phase-locked loop according to the invention;

Drawing Description Text (12):
FIGS. 21 to 25 inclusive show more detailed diagrams of second, third, fourth, fifth and sixth embodiments, respectively, of the phase-locked loop according to the invention.

Detailed Description Text (2):
The diagram shown in FIG. 1 of a phase-locked loop (PLL) according to the invention comprises, in series, a phase detector 1, a control signal generator circuit 2, a controlled oscillator 3 and an auxiliary circuit 4. The phase detector 1 delivers an output signal i to the control signal generator circuit 2, which delivers an oscillator control signal c to the controlled oscillator 3 which delivers an output signal a having a frequency f.sub.a controlled by the oscillator control signal c to the auxiliary circuit 4, which delivers two output signals d1, d2 to the phase detector 1. The phase detector 1 furthermore receives a reference signal r having a reference frequency f.sub.r from outside the loop, for example from a reference signal source 5, whose type is dependent on the application of the loop. Which of the abovementioned signals i, c, a, d1, d2 is regarded as output signal of the loop is also dependent on the application of the loop.

Detailed Description Text (3):
If the control signal generator circuit 2 in FIG. 1 were to consist of a loop filter and the phase detector 1 were to receive only one of the signals d1, d2, the configuration shown in FIG. 1 would be a configuration of a known phase-locked loop. In such a loop, the phase detector 1 compares a phase difference between the reference signal r and another input signal of the phase detector 1 and delivers an output signal which is dependent thereon and which is converted by the loop filter into an oscillator control signal for the controlled oscillator having a level which is such that the said phase difference is set to a predetermined value. The predetermined value of the phase difference is fixed by the chosen type of phase detector. In the case of some types of phase detector, the averaged level of the output signal as seen over a number of cycles of the reference signal is, in addition, dependent on the occurrence of a difference between the reference frequency f.sub.r and the frequency of the other input signal of the phase detector, the loop being designed in such a way that said frequency difference is minimized. In that case, the generally so-called creeping capture occurs for a large initial frequency difference. As the frequency difference becomes smaller, the loop enters the so-called immediate capture range of the loop in which capture range the phase difference is rapidly minimized. If the frequency difference is zero and the phase difference has the predetermined value, the loop is so-called locked ("in-lock").

Detailed Description Text (4):
The object of the invention is to provide an improved phase-coupled loop in which rapid capture occurs even in the case of a large frequency difference and the operation is not disturbed by a ripple in the output signal of the phase detector in the locked state of the loop, nor by parasitic ("spurious") signals which may occur as a consequence of different inertias and different switching characteristics of logic elements, nor by a dead zone of the transfer characteristic of the phase detector which could cause increased phase noise.

Detailed Description Text (11):
The phase detector 1 comprises, as shown in FIG. 3, an analog subtracter 18 which subtracts the first combination signal e1 from the second combination signal e2 and which delivers an output signal p (voltage) to a voltage/current converter 19. The converter 19 delivers an output signal q (current) to a limiter 20 which limits an output current i of the latter to .+-.i.sub.max. The limiter 20 is not necessary for the application of the principle of the invention. The output signal i of the limiter 20 also forms the output signal i of the detector 1, whose waveform is, in the exemplary embodiment explained here, equal to the waveform of the output signal p of the subtracter 18. The averaged value of the output signal i of the detector for a phase difference 74 and viewed over one cycle time of the reference signal r is indicated by j or i.

Detailed Description Text (18):
If it were true that N.sub.d =0, the transfer characteristic f(.theta.) shown in FIG. 5 would be obtained. In the case of FIG. 5, although the averaged value <j> of the output current i of the detector 1 is greater, in the event of a frequency difference between the input signals of the detector 1, than in the case of FIG. 6 and said greater value would be capable of resulting in a more significant control signal c, the characteristic is, as can be seen in FIG. 5, symmetrical with respect

to .theta.=0 for .theta.<0 and .theta.>0, so that the loop is unable to respond in the desired manner to a phase difference around .theta.=0 in the capture range. The equilibrium point will finish up at .theta.=90.degree. just as in the known PLL having a phase detector which comprises a single OR or exclusive OR gate. The drawback of this is that the equilibrium point is j=i.sub.max /2 and <j>=i.sub.max /2, as a result of which the detector provides, in the locked state ("in-lock"), an output signal having a pulsed form with a frequency which is twice the reference frequency and whose pulse width is equal to 1/4 of the cycle of the reference signal. In the locked state, or quiescent state, of the loop, a strongly pulsating output signal having a high frequency is thus delivered by the detector, these pulses forming the so-called ripple of the output signal of the detector in the locked state, in which state the control signal for the oscillator has a quiescent level. Because the pulses have a high energy content, they have a strongly interfering effect on the frequency stability of the output signal of the oscillator. Because the equilibrium point is given by a point half way up the slopes of the triangular transfer characteristic of the detector for the locked state of the loop, the output signal of the detector is independent of a frequency difference between the input signals of the detector as viewed over a number of cycles of the reference signal, all the phase differences between the input signals of the detector being traversed. Or, in other words, the averaged output signal of the detector is, as seen over a number of cycles of he reference signal, independent of a frequency difference between the input signals of the detector. In the case of a frequency difference between the input signals of the detector which is wide with respect to the loop bandwidth, the capture will take place slowly or in a creeping manner, which is very undesirable for many applications of the phase-locked loop.

Detailed Description Text (22):
FIG. 10 shows a more detailed diagram of a first embodiment of the phase-locked loop according to the invention. The control signal generator 2 shown in the diagram of FIG. 10 comprises a switch 22 which receives the output signal i (current) of the phase detector 1 and a control signal-return signal -Ir (a negative current). The switch 22 also receives a return control signal z as output signal of a comparator 23. The switch 22 provides an output signal u (current) to a loop filter 24 which provides an output signal v (voltage) to a voltage/current converter 25 which delivers an output signal w (current) whose proportional components x, y are delivered to a limiter 26 and to the comparator 23, respectively. As an alternative to the converter 25, a voltage/current converter could be used which does not deliver a common output signal w but which delivers via separate internal paths thereof the signals x and y for the limiter 26 and the comparator 23, respectively.

Detailed Description Text (25):
It is assumed that, if a frequency difference occurs between the reference signal r and the other input signals d1 and d2, the phase characteristic f(.theta.) of the detector 1 delivers an output signal i whose averaged value <j> is positive (see, for example, FIG. 6 for N.sub.d =1/6), that, with an increasing level of the input signal u (current) of the loop filter 24, its output signal v (voltage) increases and that the output signal w (current) of the converter 25 and the derived signals x and y, the oscillator control signal c and the frequency of the oscillator output signal a increase in harmony therewith. Under these conditions, the choice I1>I2 is valid.

Detailed Description Text (27):
It is assumed that the initial frequency f.sub.a of the output signal a of the oscillator 3 is higher at time zero than a desired frequency f.sub.w of N=N1.times.N2 (in the example, six) times the reference frequency ft (f, is, for example, 480 MHz) and that the loop is in the first state, the loop filter 24 receiving the pulse-type output signal i from the detector 1. In response to the received pulse-type input current i, the loop filter 24 will deliver a flattened voltage v which will increase as a consequence of the frequency difference present between the first and second input signals r, d1 of the phase detector 1. As a result, the converter 25 will deliver an increasing current w and the limiter 26 will also deliver a control current c which increases with time. When the comparator 23 detects that the current derived from the converter 25 goes above the first reference level I1, the return control signal z from the comparator 23 actuates the switch 22 so as to set the loop to the second state to allow the return current -Ir

through the switch 22 to the loop filter 24 instead of the output current i of the detector 1. The said initial state of the loop is shown in FIG. 12 at t=0 and the instant mentioned last at which the loop goes from the first to the second state occurs in FIG. 12 at t=500 ns. At that instant, the output signal a of the oscillator 3 has a maximum frequency f.sub.max. In the second state, the loop filter 24 receives the return current -Ir, as a result of which the output current w of the converter 25 and the oscillator control current c from the limiter 26 will decrease. If the current x reaches the relatively low third reference level I3, the limiter 26 limits the oscillator control current c to this level. At that instant, the output signal a of the oscillator 3 has a minimum frequency f.sub.max, which is lower than the desired frequency f.sub.w. If, at this same instant, or only after the output current w of the converter 25 has decreased further (as a result of which the characteristic of FIG. 12 has a (short) horizontal lowermost section), the input current y of the comparator 23 reaches the second reference level I2, the return control signal z from the comparator 23 actuates the switch 22 so as to allow the output current i of the detector 1 through again to the loop filter 24 instead of the return current -Ir and so as thereby to set the loop back to the first state. This switching point occurs in FIG. 12 at approximately the time t=1.3 .mu.s.

Detailed Description Text (28):
After setting the loop back from the second state to the first state, the output current i of the detector 1 will, as a consequence of the frequency difference still present (but with another sign) and the still positive averaged value <i> of said current i, increase the output current w of the converter 25 and the level of the oscillator control current c again until the immediate capture range of the loop is reached, for which region the frequency f, of the output signal a of the oscillator 3 is equal to or virtually equal to N.times.f.sub.r. This situation is reached in the example of FIG. 12 at approximately t=1.7 .mu.s.

Detailed Description Text (30):
The first embodiment shown in FIG. 10 of the loop according to the invention is relatively simple in that a relatively simple switch 22 and the constant return current -Ir are used. Viewed over a number of different initial situations, this embodiment gives a more rapid reaching of the immediate capture range of the loop than known phase-locked loops. However, a phase-locked loop which, even when viewed over different initial situations, can reach the immediate capture range of the loop still more rapidly can be obtained by a few changes to the diagram of FIG. 10. FIGS. 21 to 25 inclusive show second to sixth embodiments, inclusive, of the loop according to the invention, with which this more rapid capture can be achieved. Their general operation will first be explained by reference to FIGS. 13 to 20 inclusive. FIGS. 13 to 20 inclusive show the oscillator frequency f.sub.a as a function of time. In FIGS. 13, 15, 17 and 19, the initial oscillator frequency f.sub.a is between the minimum oscillator frequency f.sub.MIN and the desired oscillator frequency f.sub.w. In FIGS. 14, 16, 18 and 20, the initial oscillator frequency f.sub.a is between the desired oscillator frequency f.sub.w and the maximum oscillator frequency f.sub.max. In each of the FIGS. 13 to 20 inclusive, the time is indicated at which the desired oscillator frequency f.sub.w is reached after starting from the initial situation. This time is indicated in FIGS. 13 to 20 inclusive by t.sub.13, t.sub.14, t.sub.15, t.sub.16, t.sub.17, t.sub.18, t.sub.19 and t.sub.20, respectively.

Detailed Description Text (31):
FIGS. 13 and 14 apply to the operation of the first embodiment, explained by reference to FIG. 10, of the phase-locked loop according to the invention. The time in which the switch 22 allows the return current -Ir through instead of the output current i of the phase detector 1 is the return time (or return time) T.sub.ref. During the return time T.sub.ret, the output signal i of the phase detector 1 has no influence on the operation of the loop, as a result of which said time T.sub.ref can be regarded as lost for the rapid reaching of the desired oscillator frequency f.sub.w.

Detailed Description Text (34):
If the initial oscillator frequency f.sub.a is not equal to the desired oscillator frequency f.sub.w, the initial oscillator frequency f.sub.a has, in 50% of the cases, a value which results in the oscillator frequency f.sub.a being repelled

further from the desired oscillator frequency f.sub.w. These situations are shown in FIGS. 14, 15, 19 and 20. In the situations of FIGS. 19 and 20, however, the time loss of the return time T.sub.ret does not occur, so that it can be stated globally for all the initial situations (leaving f.sub.a =f.sub.w out of consideration) that, in the case of an operation according to FIGS. 17 to 20 inclusive, a time gain of the magnitude of the return time T.sub.ret can be achieved in 50% of the cases, in other words, that the phase-locked loop reaches the immediate capture range in a time T.sub.ret which is more rapid in the embodiment according to FIGS. 10 and 13 to 16 inclusive.

Detailed Description Text (35):
FIG. 21 shows a more detailed diagram of a phase-locked loop according to the invention. The diagram of FIG. 21 differs from the diagram of FIG. 10 in that the control signal generator circuit 2 is replaced by the control signal generator circuit 40 having an analog inverter 41 which receives the output signal i of the phase detector 1, inverts its polarity and delivers to the switch 22 the output signal -i obtained in this process instead of the return current -Ir of FIG. 10.

Detailed Description Text (36):
FIG. 22 shows a diagram of a third embodiment of the phase-locked loop according to the invention. The diagram of FIG. 22 has a control signal generator circuit 50 which differs from the control signal generator circuit 2 of FIG. 10 in that the switch 22 is omitted and the input signal u of the loop filter 24 is formed by the output signal i of the phase detector 60 of FIG. 22. The phase detector 60 differs from the phase detector 1 of FIG. 10 in that a first controlled inverter in the form of an exclusive OR gate 61 is provided in the path of the first combination signal e1 and in that a second controlled inverter in the form of an exclusive OR gate 62 is provided in the path of the second combination signal e2. The first controlled inverter 61 receives the output signal of the exclusive NOR gate 14 and the return control signal z from the comparator 23. The second controlled inverter 62 receives the output signal of the exclusive NOR gate 15 and the return control signal z from the comparator 23. Depending on the logic state of the output signal of the comparator 23, the controlled inverters 61 and 62 will invert he output signal of the exclusive NOR gate 14 or of the exclusive NOR gate 15, respectively, or in other words, they will invert the actual first and second combination signals e1 and e2, respectively. During the inversion, the polarity of the output signal p of the subtracter 18 will invert and therefore ultimately also the output signal i of the phase detector 60 and of the input signal u of the loop filter 24.

Detailed Description Text (38):
The specific duty cycle N.sub.d mentioned above can be defined more precisely for the text below by the duty cycle of a waveform which is obtained if the first and second comparison signals d1, d2 are combined by means of an exclusive OR function. With this in mind, it also appears possible to arrange for the input signal u of the loop filter 24 to invert in polarity on reaching an extreme oscillator frequency f.sub.min or f.sub.max by complementing said duty cycle N.sub.d (with respect to one). This can be achieved in a relatively simple manner with each of the diagrams, shown in FIGS. 23, 24 and 25, of fourth, fifth and sixth embodiments, respectively, of the phase-locked loop according to the invention.

Detailed Description Text (44):
Of importance for the diagrams of FIGS. 24 and 25 is the fact that the transit times of the first and second comparison signals d1, d2 are made as equal as possible, starting from the output signal b of the first divider 8. The smaller the transit time difference is, the fewer undesirable parasitic ("spurious") signals which could undesirably disturb the behaviour of the phase-locked loop will occur.

Detailed Description Text (45):
If the phase-locked loop according to the invention is virtually locked and small variations in the phase difference 74 occur in the input signals of the detector, one of which is the reference signal r, the detector 1 delivers an output signal i with narrow pulses having a fundamental frequency of 2f.sub.r. If the loop is locked, that is to say the frequency difference between the input signals of the phase detector is zero and the predetermined phase difference (in particular, zero) has been reached between said signals, such pulses may occur in the output signal i

of the detector as a consequence of inertias, finite switching times and instability of said times of logic elements of the loop. Said pulses, which are parasitic ("spurious") pulses, are, however, very narrow. Although said pulses are filtered by the loop filter, they could cause unwanted parasitic signals in the frequency spectrum of the oscillator 3 which are situated at intervals equal to a multiple of 2f, of the desired oscillator frequency. Parasitic signals having a fundamental frequency of f.sub.r, may also occur as a result of imbalance in he operation of the detector. However, parasitic signals having a frequency lower than f.sub.r, (subharmonic) will never occur. The amplitude of the parasitic signals in the frequency spectrum of the oscillator 3 becomes smaller, the smaller the width of the parasitic pulses is. The width of the pulses having repetition frequencies f.sub.r, and 2f.sub.r, is inversely proportional to the loop gain of the loop and therefore inversely proportional to a gain factor of an amplifier which is incorporated in the loop and which may be situated in the example in the loop filter 24 and/or the converter 25. As a result, the width of the pulses originating from the phase detector 1 will approach zero for a loop gain of the loop approaching infinity, as a result of which parasitic signals will no longer be present in the frequency spectrum of the oscillator 3. It is therefore preferable that the gain factor of the said amplifier is chosen as high as possible.

CLAIMS:

1. Phase-locked loop, comprising, in series, a phase detector, a control signal generator circuit having a loop filter, and a controlled oscillator which delivers an oscillator output signal having oscillator frequency (f.sub.a) between two extreme oscillator frequencies (f.sub.min, f.sub.max), a first input of the detector receiving from outside the loop a reference signal having a rectangular waveform with a reference frequency (f.sub.r) and with a duty cycle between the values zero and one, a second input of the detector receiving a first comparison signal derived from the oscillator output signal and having the same form as the reference signal, the detector operating at coincidence or noncoincidence of input signals it receives, the detector deriving a first combination signal by performing a logic combination function for the reference signal and the first comparison signal, the detector delivering an output signal, dependent on the first combination signal of the detector and the detector and the control signal generator circuit being designed so that, with no frequency difference and with a phase difference between the reference signal and another input signal of the phase detector with the loop operating in a state with an immediate capture range of the loop, the control signal generator circuit delivering a control signal to the oscillator which is suitable for setting the phase difference to a predetermined valve operating in a locked state having a predetermined quiescent value of the oscillator control signal after reaching the predetermined phase difference, characterized in that an auxiliary circuit is provided between the oscillator and the detector to receive the output signal of the oscillator and to deliver to the detector the first comparison signal and a third input signal the third input signal is such that if it were to be combined by means of an exclusive OR function with the first comparison signal a waveform results which has twice the frequency of the first comparison signal and a specific duty cycle (N.sub.d) which differs from the duty cycle of the waveform of the reference signal the detector has a third input for receiving the third input signal the detector derives from input signals received from the auxiliary circuit a second combination signal having the waveform with the specific duty cycle (N.sub.d), the detector has a subtracter circuit which subtracts the first combination signal in an analog manner from the second combination signal the output signal of the detector is determined by the difference determined by the subtracter the control signal generator circuit generates at a frequency difference between the reference signal and another input signal of the phase detector an averaged value of the output signal the detector as seen over a number of cycles of the reference signal which is not equal to a value associated with the quiescent value of the oscillator control signal and at the same time alters the oscillator control signal to arrange for the oscillator frequency (f.sub.a) to be altered by the oscillator and the control signal generator circuit adjusts the loop on reaching one extreme oscillator frequency and, in doing so, alters the oscillator control signal so that the oscillator frequency (f.sub.a) is driven in an opposite direction to the other extreme oscillator frequency.

2. Phase-locked loop according to claim 1, characterized in that the loop filter has a transfer characteristic containing an integrating term.

3. Phase-locked loop according to claim 1, characterized in that the auxiliary circuit is a phase shift circuit.

4. Phase-locked loop according to claim 3, characterized in that the phase shift circuit has a series of gates which receives the first comparison signal and which delivers a second comparison signal delayed with respect thereto as third input signal to the detector.

5. Phase-locked loop according to claim 1, characterized in that the auxiliary circuit comprises dividers which divide the output signal of the oscillator and logically combine output signals thereof to form the first and second comparison signals.

6. Phase-locked loop according to claim 5, characterized in that a first divider of the auxiliary circuit divides the output signal of the oscillator by a first factor (N1), a logic circuit of the first divider combines internal signals thereof to form an output signal of the first divider having the specific duty cycle (N.sub.d), and a second divider of the auxiliary circuit divides a signal derived from the oscillator output signal by a second factor (N2) in order to deliver an output signal which determines the first comparison signal the oscillator frequency (f.sub.a) being, in the locked state of the loop, equal to the product of the reference frequency (f.sub.r), the first factor (N1) and the second factor (N2) (f.sub.a =f.sub.r N1 N2).

7. Phase-locked loop according to claim 6, characterized in that the auxiliary circuit has an inverter which receives the output signal of the first divider having the specific duty cycle (N.sub.d) and which delivers the third signal as second combination signal to the detector.

8. Phase-locked loop according to claim 6, characterized in that the auxiliary circuit has a third division derived from the oscillator output signal having the specific duty cycle (N.sub.d) by the second factor (N2), the third divider switches at edges of the oscillator output signal having the specific duty cycle (N.sub.d) other than edges at which the second divider switches, and the third divider delivers the second comparison signal.

9. Phase-locked loop according to claim 1, characterized in that the control signal generator circuit has, in addition to the loop filter a comparator, an input of the loop filter is coupled to an output of the phase detector, a signal derived from the output signal of the loop filter determines the output signal of the control signal generator circuit as oscillator control signal, the comparator receives a third comparison signal derived from the output signal of the loop filter and two reference levels inverter means are provided in the loop, and in that, if the third comparison signal exceeds one of the two reference levels in a direction starting from the other reference level, an output signal of the comparator as return control signal activates the inverting means in order to invert one or more signals received by the inverter means and in order thereby to invert the polarity thereby of the input signal of the loop filter.

10. Phase-locked loop according to claim 9, characterized in that the inverter means comprise means, connected in a signal path between the subtracter and the loop filter for inverting the polarity of the input signal of the loop filter in response to the return control signal.

11. Phase-locked loop according to claim 10, characterized in that the inverting means comprise a switch connected between the phase detector and the loop filter and a source, connected to the switch of a control signal-return signal having constant level and having a polarity which is opposite to a polarity of the output signal of the detector in the event of a frequency difference between the input signals of the detector as viewed over a number of cycles of the reference signal and the switch allows the output signal of the detector or the return signal through to the loop filter in response to the return control signal.

12. Phase-locked loop according to claim 9, characterized in that the inverting means comprise a switch connected between the phase detector and the loop filter and an inverter which is connected between the switch and the phase detector and which inverts the polarity of the output signal of the detector, and the switch allows the output signal of the detector or the output signal of the inverter through to the loop filter in response to the return control signal.

13. Phase-locked loop according to claim 9, characterized in that the inverting means comprise first and second controlled inverters in the paths of the first and second combination signals, respectively, and the inverters invert or do not invert the first and second combination signals, respectively, in response to the return control signal.

14. Phase-locked loop according to claim 9, characterized in that the inverter means complement the current specific duty cycle (N.sub.d) in response to the return control signal.

15. Phase-locked loop according to claim 14, characterized in that the inverter means comprise a controlled inverter in the path of the first comparison signal and the inverter inverts or does not invert the first comparison signal in response to the return control signal.

16. Phase-locked loop according to claim 8, characterized in that the control signal generator circuit has, in addition to the loop filter, a comparator, an input of the loop filter is coupled to an output of the phase detector a signal derived from the output signal of the loop filter determines the output signal of the control signal generator circuit as oscillator control signal, the comparator receives a third comparison signal derived from the output signal of the loop filter and two reference levels, inverter means are provided in the loop, and in that, if the third comparison signal exceeds one of the two reference levels in a direction starting from the other reference level, an output signal of the comparator as return control signal activates the inverting means in order to invert one or more signals received by the inverter means and in order thereby to invert the polarity thereby of the input signal of the loop filter

wherein said phase-locked loop is further characterized in that the inverter means complement the current specific duty cycle (N.sub.d) in response to the return control signal; and

wherein said phase-locked loop is further characterized in that the inverting means comprise a controlled inverter between the output of the first divider and the inputs of the second and third dividers the second divider and the third divider switching at edges, going in opposite directions, of their common input signal, and the inverter inverting or not inverting the output signal of the first divider in response to the return control signal.

17. Phase-locked loop according to claim 8,

characterized in that the control signal generator circuit has, in addition to the loop filter, a comparator an input of the loop filter is coupled to an output of the phase detector a signal derived from the output signal of the loop filter determines the output signal of the control signal generator circuit as oscillator control signal, the comparator receives a third comparison signal derived from the output signal of the loop filter and two reference levels, inverter means are provided in the loop, and in that, if the third comparison signal exceeds one of the two reference levels in a direction starting from the other reference level, an output signal of the comparator as return control signal activates the inverting means in order to invert one or more signals received by the inverter means and in order thereby to invert the polarity thereby of the input signal of the loop filter

wherein said phase-locked loop is further characterized in that the inverter means complement the current specific duty cycle (N.sub.d) in response to the return control signal; and

wherein said phase-locked loop is further characterized in that the inverting means comprise first and second controlled inverters between the output of the first divider and the input of the second divider and the input of the third divider, respectively, the inverters being of different types which deliver inverted signals with respect to one another, the second divider and the third divider switching at edges, going in the same direction, of their respective input signals and the inverters inverting or not inverting the output signal of the first divider in response to the return control signal.

18. Phase-locked loop according to claim 1, characterized in that the control signal generator circuit has at its output a limiter which limits the control signal it delivers to a third reference level.

19. Phase-locked loop according to claim 1, characterized in that the control signal generator circuit has an amplifier connected to the output side of the loop filter and having a high gain factor to amplify the output signal of the loop filter.

20. Phase-locked loop according to claim 6 to inclusive, characterized in that the lowest (f.sub.min) of the extreme frequencies (f.sub.min, f.sub.max) is greater than the total division factor (N=N1.multidot.N2) divided by two, times the reference frequency (f.sub.r) (f.sub.min>N/ 2.multidot.f.sub.r).

21. Phase-locked loop according to claim 1, characterized in that the oscillator is a current-controlled oscillator, and the detector and the control signal generator circuit have means which deliver currents as input signals to one or more of: a present switch a comparator a limiter, and the oscillator.

22. A phase-locked loop comprising:

a phase detector having a first input for receiving a reference signal having a frequency f.sub.r, a second input for receiving a first auxiliary circuit output signal, and a third input for receiving a second auxiliary circuit output signal, and in response to the first, second and third inputs, generating a detector output signal;

a control signal generator circuit for receiving said detector output signal and generating an oscillator control signal; and

an oscillator for receiving said oscillator control signal and generating an oscillator output signal having an oscillator frequency f.sub.a ; and

an auxiliary circuit for receiving said oscillator output signal and for generating said first auxiliary circuit output signal and said second auxiliary circuit output signal by dividing said oscillator output signal.

23. The phase-locked loop according to claim 22, wherein the auxiliary circuit comprises:

a first divider for dividing the oscillator output signal by a first factor of N1 to generate a first divider output signal;

a second divider for dividing the first divider output signal by a second factor of N2, the second divider generating a second divider output signal; and

a third divider for dividing the first divider output signal by said second factor of N2, the third divider generating a third divider output signal.

24. The phase-locked loop according to claim 23, wherein the second divider output signal provides the first auxiliary circuit output signal, and the third divider output signal provides the second auxiliary circuit output signal.

25. The phase-locked loop according to claim 23, wherein the second divider and the third divider switch at different edges of their respective input signals.

26. The phase-locked loop according to claim 23, wherein the oscillator frequency

f.sub.a is equal to the product of the reference frequency f.sub.r , the first factor N1 and the second factor N2 in the locked state of the loop.

27. The phase-locked loop according to claim 22, wherein the auxiliary circuit comprises:

a first divider for dividing the oscillator output signal by a first factor of N1 to generate a first divider output signal;

a second divider for dividing the first divider output signal by a second factor of N2, the second divider generating a second divider output signal; and

an inverter for inverting the first divider output signal to generate an inverter output signal.

28. The phase-locked loop according to claim 27, wherein the second divider output signal provides the first auxiliary circuit output signal, and the inverter output signal provides the second auxiliary circuit output signal.

29. The phase-locked loop according to claim 22, wherein the phase detector further comprises:

a first combination logic circuit for receiving said reference signal and said first auxiliary circuit output signal, and generating a first combination logic circuit output; and

a second combination logic circuit for receiving said first auxiliary circuit output signal and said second auxiliary circuit output signal, and generating a second combination logic circuit output.

30. The phase-locked loop according to claim 29, wherein said first and second combination logic circuits comprises exclusive OR gates.

31. The phase-locked loop according to claim 29, wherein said phase detector further comprises:

a subtracter for receiving said first combination logic circuit output and said second combination logic output, for determining the difference therebetween, and for generating a subtractor output signal indicative of said difference.

32. The phase-locked loop according to claim 22, wherein said control signal generator circuit includes:

a loop filter for receiving an input based on the phase detector output signal, and for generating a loop filter output signal; and

a comparator for receiving an input based on the output of said loop filter, and for generating a return control signal, said comparator also receiving a first and a second reference signals, said comparator determining whether said input based on the output of said loop filter exceeds one of the two reference signals.

33. The phase-locked loop according to claim 32, further including:

an inverter located in the loop for receiving said return control signal from said comparator, and for inverting an input based on the return control signal.

34. The phase-locked loop according to claim 33, wherein said inverter is interposed between said phase detector and said loop filter, and wherein said inverter inverts the polarity of the input signal of the loop filter in response to the return control signal.

35. The phase-locked loop according to claim 34, wherein the inverter comprises a switch having a first input connected to an output of the phase detector, and having a second input connected to a control signal-return signal having a constant level and having a polarity which is opposite to a polarity of the output of the phase

detector, and wherein the switch selects between the first input and the second input based on the return control signal.

36. The phase-locked loop according to claim 34, wherein the inverter comprises a switch having a first input connected to an output of the phase detector, and having a second input connected to the output on a signal inverter, wherein the signal inverter inverts the output of the phase detector, and wherein the switch selects between the first input and the second input based on the return control signal.

37. The phase-locked loop according to claim 33, further comprising:

a first combination logic circuit for receiving said reference signal and said first auxiliary circuit output signal, and generating a first combination logic circuit output; and

a second combination logic circuit for receiving said first auxiliary circuit output signal and said second auxiliary circuit output signal, and generating a second combination logic circuit output;

wherein the inverter comprises a first and second inverters for inverting the first combination logic circuit output and the second combination logic circuit output, respectively, wherein the first and the second inverters invert the first and second combination logic circuits outputs based on the return control signal.

38. The phase-locked loop according to claim 33, wherein the auxiliary circuit comprises:

a first divider for dividing the oscillator output signal by a first factor of NI to generate a first divider output signal;

a second divider for dividing the first divider output signal by a second factor of N2, the second divider generating a second divider output signal; and

a third divider for dividing the first divider output signal by said second factor of N2, the third divider generating a third divider output signal.

39. The phase-locked loop according to claim 38, wherein the inverter receives the second divider output signal and inverts this signal based on the return control signal.

40. The phase-locked loop according to claim 38, wherein the inverter receives the first divider output signal and inverts this signal based on the return control signal.

41. The phase-locked loop according to claim 38, wherein the inverter comprises a first and second inverters which respectively invert the inputs to the second and third dividers based on the return control signal.

42. The phase-locked loop according to claim 22, wherein the oscillator comprises a current controlled oscillator.